Manufacturable Parasitic-Aware Circuit-Level FETs in 65-nm SOI CMOS Technology

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***Abstract*—This letter reports the statistical analysis of circuit-level FET high-speed performance in 65-nm silicon-on-insulator CMOS technology. Practical performance metrics are derived from full 300-mm wafer measurements. The proposed circuit-level layout wiring parasitics-aware FET reflects realistic FET that is placed in circuits. Its measurement and model are directly applicable to circuit design in conjunction with multiple layers of yield and manufacturability considerations. A stretched gate-pitch NFET design shows an average current gain cutoff frequency f_T of 250 GHz, with 7.6% standard deviation, 6.7% mismatch standard deviation, and maximum f_T of 307 GHz. The proposed characterization methodology will become more relevant to technologies beyond 65 nm.**

***Index Terms*—Circuit-level FET with wiring parasitics, current gain cutoff frequency f_T, FET yield and manufacturability, full 300-mm wafer statistical analysis, 65-nm silicon-on-insulator (SOI) CMOS.**

I. Introduction

SILICON-ON-INSULATOR (SOI) CMOS technology has been a breakthrough for high-performance system-on-chip manufacturing [1], and the 65-nm SOI FET devices have been reported to have more than 300-GHz current gain cutoff frequency f_T [2]. As technology develops, die-to-die variation within a wafer becomes as important as wafer-to-wafer variation [3]. In this letter, the die-to-die variation of circuit-level FET high-speed performance is investigated through a 300-mm wafer in 65-nm SOI. The resulting statistical analysis represents realistic performance metrics. It is important to have a FET characterization methodology that is aware of the wiring resistance and capacitance that originate from first-hand back-end-of-line (BEOL) layout. This letter demonstrates a circuit-level FET design and characterization that includes contacts, vias, and metal wires in the device under test (DUT). By including wiring parasitics, a layout for circuit-level FET needs optimization that is specific to the given technology. The optimization targets are not only performances, such as device g_m, f_T, and f_{max}, but also DUT physical and functional yield. The circuit-level FET performance is further exploited by layout optimization. For example, FET gate to diffusion contact distance is stretched by a factor. The proposed circuit-level layout-optimized FET measurement manifests practical circuit performance with statistics. Its yield and manufacturability are improved through the layout optimization. High-speed mixed-signal components will benefit from enhanced performance and statistical model of the proposed layout-optimized circuit-level FETs.

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II. Layout-Optimized Circuit-Level FET Characterization

The increasing site-to-site device variation across a wafer in sub-100-nm semiconductor technology has necessitated statistical method to characterize device performance. With regard to FET device, technologies have been evaluated through common metrics, such as f_T and f_{max}. So far, maximum performances have been published for benchmarking purpose [2], [4]–[7]. Due to increasing process variation, practical circuit performance metrics are required, and they should be provided as statistics. Besides, the characterized FETs have been device-level FETs, where unnecessary wiring parasitics are deembedded. However, it does not relate to realistic device manufacturability, physical yield, performance, and modeling. In sub-100-nm technologies, FET performance is becoming more dependent on the neighboring layout. Therefore, both the front-end-of-line device and the first-hand BEOL layout need to be designed together in the technology development stage for yield and performance. This letter proposes a FET characterization vehicle of circuit-level FET that embraces wiring parasitics with layout optimization, as shown in Fig. 1. Included parasitics are contacts to active region and gate, vias, and first and second metal lines. The proposed circuit-level FET is defined as a rectangular area, and an open deembedding structure will be an exact rectangular-shape cut in layout view. Layout extraction is improved since stress effect and wiring parasitics are included in the model, and it is less affected by additional layout. Consequently, it will be useful to enhance model-to-hardware correlation. When both device-level FET and first-hand layout are considered as a circuit-level FET, there are several ways to optimize the layout. One of the strategies to increase performance is FET gate-pitch stretching.

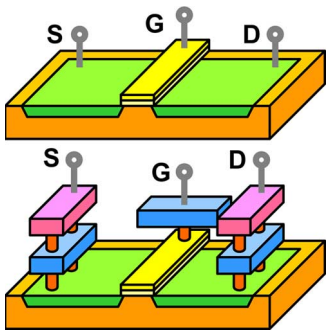

Fig. 1. Diagrams for device-level FET device with complete deembedding (top) and proposed circuit-level FET device with wiring parasitics (bottom).

TABLE I
CIRCUIT-LEVEL FET PROPERTIES AND STATISTICAL CHARACTERISTICS

	NFET		PFET	
Gate pitch type	Stretched	Minimum	Stretched	Minimum
Gate pitch ratio	2	1	2	1
W (μm)	40	40	40	40
Fingers	40	40	40	40
L (nm)	40	40	35	35
DUT area (μm^2)	52.2	37.1	52.2	37.1
Average f_T (GHz)	250	217	160	129
f_T standard deviation (%)	7.61	7.10	6.75	5.95
f_T mismatch (%)	6.73	4.74	6.56	5.45

By distancing diffusion contacts from the gate, parasitic capacitances are reduced, and more stress is applied though the stretched opening by a stress liner. A tradeoff of FET gate-pitch stretching is extended device layout area. In this letter, the circuit-level FET gate-pitch stretching effect is investigated with optimal contacts and via arrangements. This letter concentrates on statistical characterization of f_T for simplicity among FET parameters since it is a good representation of FET high-speed performance, and it is well defined numerically from S-parameter.

III. EXPERIMENTAL RESULTS

Four types of circuit-level FETs were implemented in 65-nm SOI CMOS technology, as arranged in Table I. Another set of FETs are placed about 14 mm away from the first set for mismatch analysis. Each circuit-level FET is 40 μm wide with 40 fingers, and gate contacts were densely populated to reduce gate resistance. The pitch spacing ratio of stretched to minimum pitch design is 2, and the DUT area ratio is about 1.41. With gate and drain dc biasings, H-parameters are obtained from the up to 50-GHz S-parameter measurement and open-short deembedding [4]. A -20 dB/dec line is fitted to $|H_{21}|$ by minimizing the root-mean-square error in the 5- to 10-GHz range, and the 0-dB crossing frequency is the current gain cutoff frequency f_T. Stretched NFET f_T change over $V_{\rm GS}$ and $V_{\rm DS}$ sweep from 0 to 1.2 V with 0.1-V steps is plotted in Fig. 2. The maximum f_T is attained with $V_{\rm GS} = 0.7$ V and $V_{\rm DS} = 1.2$ V. The f_T saturates at $V_{\rm DS} = 1.0$ V, as marked in

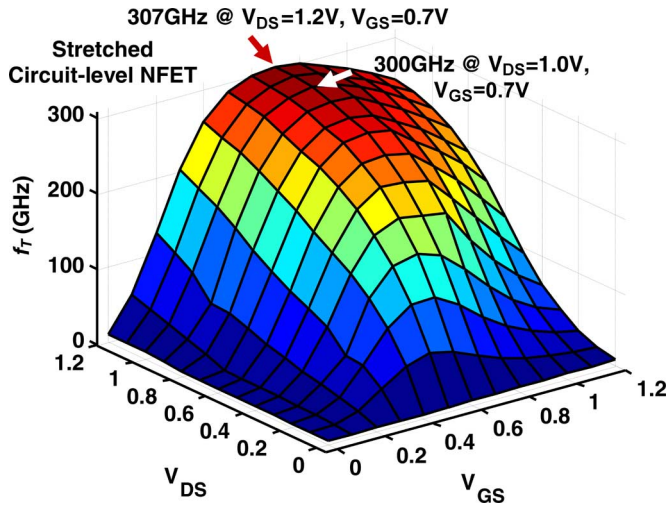

Fig. 2. Circuit-level stretched gate-pitch NFET current gain cutoff frequency f_T responses with gate voltage $V_{\rm GS}$ and drain voltage $V_{\rm DS}$ sweep from 0 to 1.2 V with 0.1-V steps. Maximum of 307 GHz is observed at $V_{\rm GS} = 0.7$ V and $V_{\rm DS} = 1.2$ V. f_T is almost saturated after $V_{\rm DS} = 1.0$ V, as marked in 300 GHz at $V_{\rm GS} = 0.7$ V and $V_{\rm DS} = 1.0$ V. The data were collected at the highest f_T performance site out of full-wafer measurements.

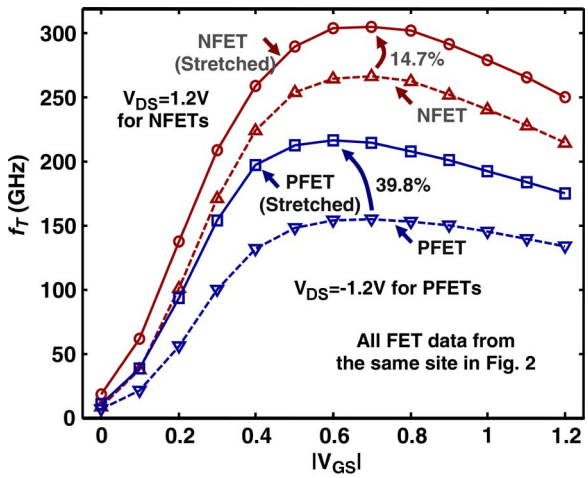

Fig. 3. Stretched and minimum gate-pitch FET f_T responses with gate voltage $|V_{\rm GS}|$ sweep from 0 to 1.2 V with 0.1-V step at $|V_{\rm DS}| = 1.2$ V. The gate-pitch stretching improves NFET f_T by 14.7% and PFET by 39.8% in this site. Stretched PFET f_T response shifts slightly to higher $V_{\rm GS}$ (to left), and the maximum f_T is sampled at $V_{\rm GS} = -0.6$ V, whereas NFET maximum f_T's are sampled at $V_{\rm GS} = 0.7$ V.

$f_T = 300$ GHz at $V_{\rm GS} = 0.7$ V. Four types of circuit-level FET f_T measurement in the same site with $|V_{\rm GS}|$ sweep at $|V_{\rm DS}| = 1.2$ V are plotted in Fig. 3. Similar tests were performed on 108 sites in a 65-nm SOI 300-mm wafer. Statistics are analyzed in Table I. On average, stretched NFET outperforms minimum pitch NFET by 15.2%, and stretched PFET gains 24.0% in f_T. NFETs have more relative variations than PFETs, and stretched FETs show more relative standard variation than minimum pitch FETs. Also, stretched FETs have more mismatch relative variation than minimum pitch FETs. Circuit-level FET f_T cross correlations are plotted in Fig. 4. The cross correlations are more than 80%, except for the PFET versus stretched NFET and stretched PFET cases. The numbers suggest that circuit-level FET f_T performances are well correlated by proximity. Also, the minimum pitch NFET can serve as a good performance

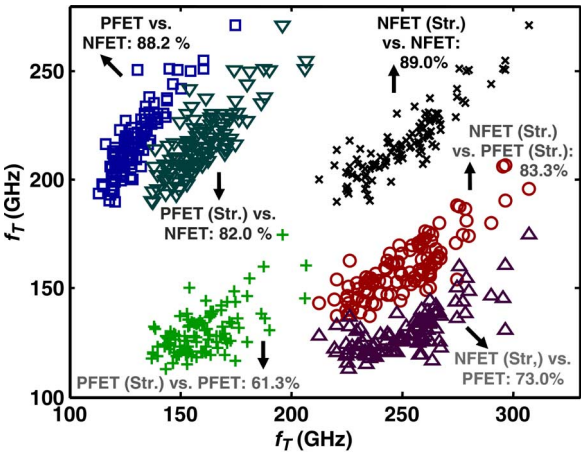

Fig. 4. Circuit-level FET f_T cross-correlation plots. High cross correlations among FETs imply that site-to-site variation changes neighboring FET performance at the same time. NFET has the highest cross correlations (89%, 82.0%, and 88.2%) to all other FETs.

representative for others since it maintains more than 80% cross correlations with all other FETs. When this work is compared with the state-of-the-art sub-100-nm CMOS device studies, the reported f_T performances are proven more manufacturable through statistical analysis than the previous works [2], [4]–[7], where only a few of maximum figures were reported. The characterized circuit-level FETs include layout resistance and capacitance for practicality. Both NFETs and PFETs are characterized. Not only the maximum but also the nominal f_T's are comparable to other works [2], [6], [7].

IV. Conclusion

The manufacturable circuit-level FETs with layout optimization were presented. The proposed FET was examined with respect to performance yield and layout optimization through statistical analysis. The methodology was applied to f_T analysis of stretched and minimum gate-pitch circuit-level NFETs and PFETs. The proposed circuit-level FET design and characterization approach will be more relevant to technologies beyond 65 nm due to increasing variation and design tool complexity.

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