Symmetric Vertical Parallel Plate Capacitors for On-Chip RF Circuits in 65-nm SOI Technology

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***Abstract*—This letter presents symmetric vertical parallel plate (VPP) capacitors in 65-nm silicon-on-insulator CMOS technology. Three VPP capacitors with different metal layer options are examined with respect to effective capacitance density and Q-factor. An effective capacitance of 2.18 fF/μm^2 and a Q-factor of 23.2 at 1 GHz are obtained from a 1x + 2x (M1–M6) metal layer configuration's pre-de-embedding measurement. VPP capacitor symmetry, mismatch, leakage current density, vertical scalability, and variation characteristics from a 300-mm wafer are discussed.**

***Index Terms*—Radio frequency (RF) passive component, vertical and horizontal scalability, vertical native back-end-of-line (BEOL) capacitor, vertical parallel plate (VPP) capacitor, 65-nm silicon-on-insulator (SOI) CMOS technology.**

I. Introduction

RF system-on-chip manufacturing requires high-quality on-chip passive devices, such as inductors and capacitors. On-chip capacitor specifications include capacitance density, voltage linearity, leakage current, mismatch, and Q-factor [1]. It has not been trivial to achieve both high Q-factor and capacitance density, and either of the two has been optimized at the expense of the other [2]–[4]. As semiconductor technology develops, the minimum definable feature size decreases, and the number of layers increases. As a result, a capacitor is built as a 3-D structure, such as vertical parallel plate (VPP) [3]–[5], as described in Fig. 1. The VPP capacitor is defined by a standard layout within existing masks, without additional processes. Q-factor is maximized with layout strategies [4], and it has symmetric characteristics by its nature. This letter reports VPP capacitor implementations in 65-nm silicon-on-insulator (SOI) CMOS technology. Three configurations with 1x, 2x, and 1x + 2x layer options are measured. The result confirms that the capacitance density of the VPP capacitor is improving over nanometer-technology generations [5] with comparable Q-factors. The VPP capacitor statistical symmetry, mismatch, vertical scalability, and variation characteristics are examined.

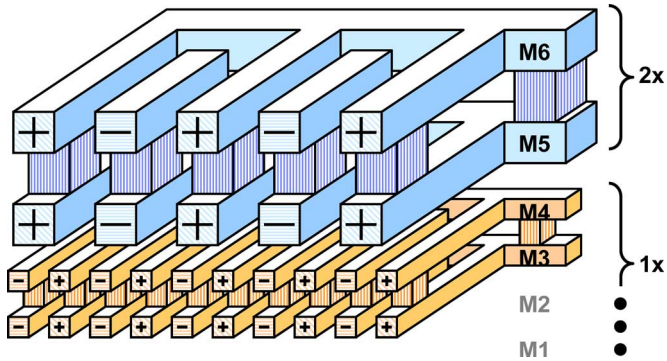

Fig. 1. VPP capacitor layout diagram. The upper two layers of the 1x layer (M3 and M4) and the 2x layers (M5 and M6) are shown. Interdigitated metal lines and interlayer vias are placed to maximize capacitance density and manufacturability.

II. VPP Capacitor Implementation

The 65-nm SOI technology offers ten metal layers with four layer thicknesses. The layer of minimum unit metal linewidth and thickness is referred to as the "1x" layer, and the upper layers are arranged as 2x, 4x, and 8x. The 1x layer provides the highest vertical plate capacitance, while it suffers from the highest line resistance, which degrades Q-factor. Its coupling to substrate serves as a path for signal leakage. The vertical implementation provides native symmetry to VPP capacitors since both nodes face substrate equally. Three VPP capacitor configurations—1x, 2x, and 1x + 2x—are implemented. The 1x-layer (M1–M4) metal line pitch is 0.24 μm, and the 2x-layer (M5 and M6) pitch is 0.64 μm. A 3-D diagram of the 1x + 2x VPP capacitor is shown in Fig. 1. Each capacitor size is 100 μm by 100 μm, and open and short (O/S) de-embedding structures are fabricated. A second set of capacitors is laid out for mismatch analysis. Vias are arranged to maximize manufacturability as a "via farm."

III. Experiment Result

The fabricated VPP capacitors' S-parameters are measured, and Fig. 2 shows the 1x + 2x capacitor's O/S de-embedded S-parameters. The S21 and S12, and S11 and S22 map to the same trace with symmetry. The capacitance density is a

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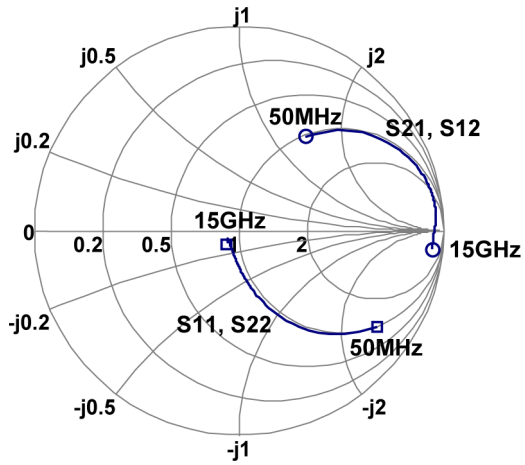

Fig. 2. VPP capacitors' S-parameter measurements Smith chart plots from 50 MHz to 15 GHz. The S21 and S12 plots are mapped on the same trace; so do the S11 and S22 parameters.

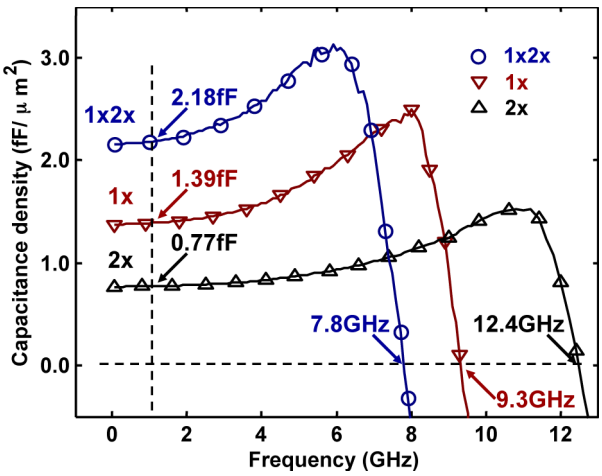

Fig. 3. Density plots of the 1x, 2x, and 1x + 2x VPP capacitances. The capacitors show capacitance densities of 1.39, 0.77, and 2.18 fF/μm^2, respectively, at 1 GHz. Each VPP is 100 μm by 100 μm. The 1x + 2x capacitance is the sum of the 1x and 2x capacitances within 1% error.

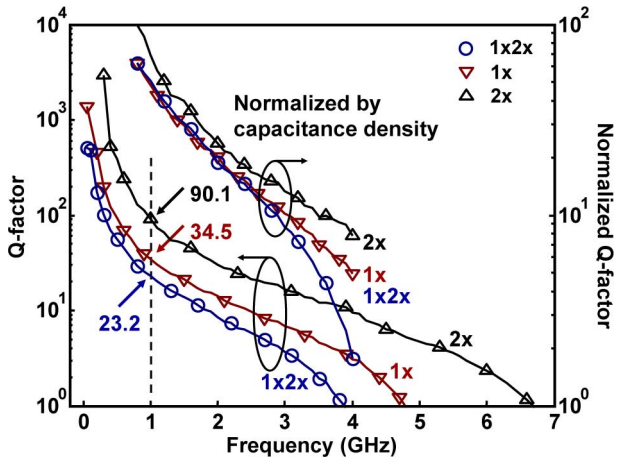

Fig. 4. VPP capacitor Q-factor plots. Q-factors are estimated from pre-de-embedding data due to singularity in the de-embedded Q-factor. The 1x, 2x, and 1x + 2x capacitors show Q-factors of greater than 34.5, 90.1, and 23.2, respectively, at 1 GHz. In the normalized Q-factor per unit capacitance plot, the 1x + 2x capacitor's Q-factor scaling effect by capacitance is observed. The normalized plots are shifted upward for visualization.

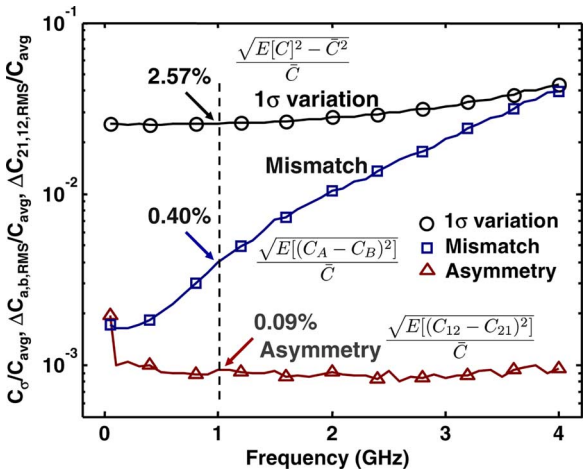

Fig. 5. Statistical characteristics of the 1x + 2x VPP capacitor. The 1σ variation is 2.57%, the rms mismatch is 0.40%, and the rms asymmetry is 0.09% at 1 GHz. The rms capacitor asymmetry is about 60 dB below the capacitance value.

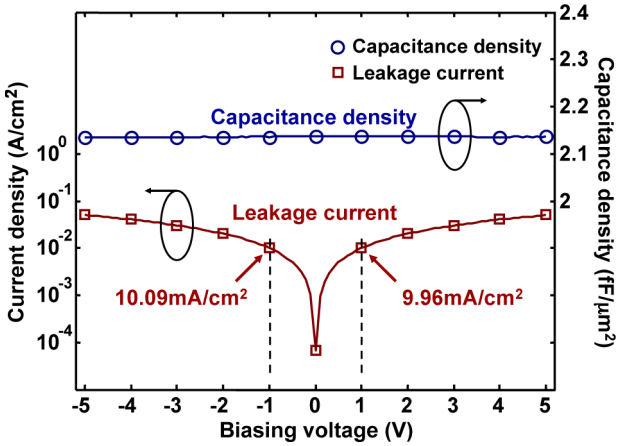

Fig. 6. Leakage current and capacitance densities with dc voltage biasing to the 1x + 2x VPP capacitor. The capacitor shows symmetric leakage current, and a current density of about 10^{-2} A/cm^2 is observed at $\pm$1 V. The capacitance density is 2.13 fF/μm^2 at 200 MHz, and its voltage linearity is less than 80 ppm/V^2.

function of frequency, as plotted in Fig. 3. The 1x, 2x, and 1x + 2x capacitors show 1.39, 0.77, and 2.18 fF/μm^2, respectively, at 1 GHz. Their threshold frequencies are 9.3, 12.4, and 7.8 GHz, respectively. A VPP capacitor turns into an inductor above the threshold frequency. The 1x + 2x capacitance is the sum of 1x and 2x capacitances within 1% error. It suggests that the VPP capacitor is vertically scalable with linearity. The 1x + 2x capacitor density is an improvement from a previous measurement of 1.76 fF/μm^2 in 0.12-μm SOI technology [5]. The Q-factors of VPP capacitors from raw S-parameter data are plotted in Fig. 4. The 1x, 2x, and 1x + 2x capacitors have Q-factors of greater than 34.5, 90.1, and 23.2 at 1 GHz. In addition, the Q-factors are normalized to unit capacitance and scaled for visibility in the plot. The Q-factor of the 1x + 2x capacitor is scaled down by higher capacitance density than the 1x capacitor. The 1x + 2x VPP capacitor's

statistics are plotted in Fig. 5. A 300-mm wafer is measured for 150 capacitors. The 1σ variation is 2.57%, and the rms mismatch is 0.40% at 1 GHz. The mismatch set is about 550 μm away from the first set. The bottom line is the rms error between port1-to-port2 and port2-to-port1 capacitances, which is normalized by average. The symmetry error is 0.09% or 60 dB below the nominal capacitance. The symmetry of the 1x + 2x VPP capacitor is also observed in the leakage current density plot in Fig. 6. A current density of about 10^{-2} A/cm^2 is observed at ± 1 V. It suggests that a VPP capacitor needs application-specific layout optimization for capacitance density, Q-factor, and leakage current. The capacitor voltage linearity is smaller than 80 ppm/V^2.

IV. Conclusion

Symmetric VPP capacitor measurements in 65-nm SOI technology were presented. The VPP capacitance density with 65-nm technology is 2.18 fF/μm^2, a 24% improvement from 0.12-μm technology. The capacitance density, quality factor, symmetry, vertical scalability, and compatibility to existing nanoscale CMOS technology place the VPP capacitor as an alternative for RF applications.

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