

Scalable Statistical Measurement and Estimation of a mmWave CML Static Divider Sensitivity in 65nm SOI CMOS

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Abstract — A CML static divider operates up to 82.4GHz with 90% yield for 0dBm input is statistically measured and estimated. The proposed method of statistical measurement enables reliable sensitivity curve estimation by 55% of standard variation, based on the analytic model, simulations, and scalable DC and RF measurements for the first time. A 300mm full wafer is scanned for the validation.

Index Terms — mmWave CML static divider, sensitivity curve, process-induced variation, scalable measurement and statistical performance estimation, 65nm SOI CMOS.

I. INTRODUCTION

The millimeter-wave (mmWave) communications system will be realized with CMOS technology in near future, as mmWave PLL and transceiver components have been demonstrated. They are implemented in the advanced CMOS processes to take advantage of the device speed, manufacturing, and SoC integration. But current sub-100nm CMOS technology entails increasingly severe process-induced variability [1]. In a PLL block diagram in Fig. 1, the variability affects the VCO and the divider that operate at mmWave frequency. Not only the active and passive components, but also the parasitic capacitances are subject to the variability. The circuit component physical dimensions are much smaller than the RF system, and the technology variability amplifies the mmWave circuit performance variation. The PLL front-end is becoming a potential bottleneck for the chip-limited yield of the entire SoC.

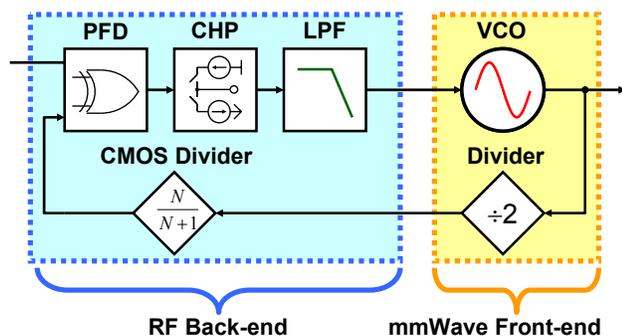


Fig. 1. A mmWave PLL block diagram. The VCO and divider operate at the carrier frequency. The front-end determines the system performance and yield under process variability.

Due to the variability, the statistical characterization of a divider is important for variation-aware design, simulation, and characterization [2-5]. The challenges are complicated test setup and measurement procedure. A divider test setup example is described in Fig. 2.

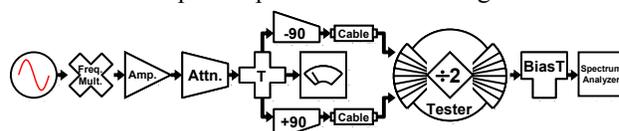


Fig. 2. A typical mmWave divider test setup diagram. The signal source, attenuator, phase shifters, power meter, and spectrum analyzer are essential for divider measurement.

The mmWave waveguide test setup is sensitive and subject to substantial signal losses in the phase shifter, waveguides, adapter, cable, probe, and contact resistance. A divider is comprehensively characterized with a sensitivity curve, which measures the minimum dividable input signal power at each frequency. The curve measurement is not trivial to automate with an algorithm. The divider output involves highly nonlinear and wide-band outputs with input-locked operation, single-balanced mixer, and self-oscillation.

The paper presents scalable divider performance estimation and validation based on the model-to-hardware correlation (MHC) and the scalable statistical DC and self-oscillation measurements. A CML divider small-signal analysis is presented in section II. A proposed estimation method is introduced with simulation results in section III. CML divider statistical measurements from a 300mm 65nm SOI CMOS wafer are used for the verification in section IV.

II. CML DIVIDER SMALL-SIGNAL ANALYSIS

A CML latch in Fig. 3 consists of a differential pair as a single-balanced mixer and a negative g_m pair. An RF input and a 180-degree complement are applied to the tail inputs. The mixer (local) modulation input and the latch output maintain a certain phase difference for steady-state operation as a divider. Analytical equations for divider characteristics and sensitivity curve are derived through a small-signal analysis of the CML latch.

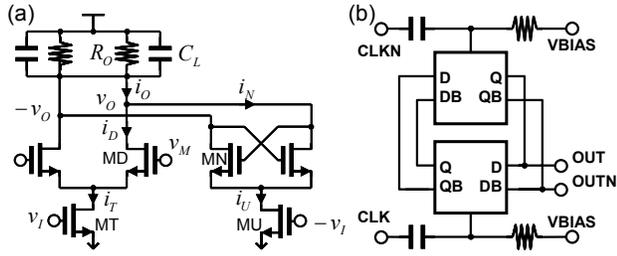


Fig. 3. (a) CML latch schematic diagram and (b) divider block diagram with AC coupling and DC bias.

The small-signal gain $\bar{g}_{M,D}$ in the different pair is modulated by the tail input v_I . It is solved through a power series expansion and an approximation as (1).

$$g_{M,D} \approx \sqrt{\beta_D I_T} \left(1 + \frac{i_I(t)}{2I_T} \right) \quad (1)$$

The negative g_m pair tail input has 180-degree shift with $-v_I$. By assuming steady state for self-oscillation and input-locked operations, v_O and v_M has 90 degrees phase difference. The mixing operations between v_I and v_M , and $-v_I$ and v_O are approximated by removing high-frequency terms [5]. A current sum equation at v_O becomes $i_O = i_N + i_D$. It is arranged as real and imaginary terms, and it becomes a circle equation, using Pythagorean trigonometric identity. By solving the minimum input A_i for the circle, the divider sensitivity curve equation is obtained as (2).

$$A_{mn}(f_{in}) \geq \frac{2\sqrt{2}}{\sqrt{\beta_D \beta_T + \beta_N \beta_U}} |G_{M,D} - \pi f_{in} C_L| \quad (2)$$

From this, several divider characteristics are derived as depicted in Fig. 4. Most importantly, it is proven that, to the first-order approximation, sensitivity curve is determined by DC parameters and the self-oscillation frequency $f_{SO} = G_{M,D}/2\pi C_L$.

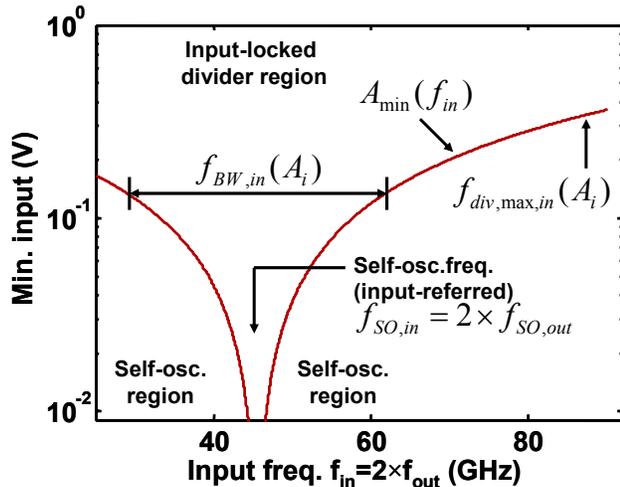


Fig. 4. The divider sensitivity curve analytic equation plot and divider characteristics.

Therefore, f_{SO} and DC measurements such as active current I_A and quiescent current I_Q are key parameters for sensitivity curve estimation. With a spectrum analyzer, f_{SO} is precisely measured in the lower frequency range. The DC and f_{SO} measurements are readily automated with scalability in testing time and setup complexity.

III. STATISTICAL ESTIMATION AND SIMULATION

Fig. 5 describes a statistical method for sensitivity curve estimation. Inputs to the estimator are f_{SO} , I_A and I_Q at $V_{BIAS}=0.6V$ and $V_{DD}=1.8V$. Outputs of the estimator are an offset and a scaling factor with respect to a nominal sensitivity curve at $V_{BIAS}=0.6V$, thus uniquely determining an individual sensitivity curve. The training for the sensitivity curve estimator involves two-step processes: 1) Based on simulation data (f_{SO} , I_A , I_Q , and sensitivity curve cut-off frequencies $f_{cut-off}$), the estimator is accordingly trained. The $f_{cut-off}$ are preferred, as sample points of a sensitivity curve, than the curve itself. It is because even a single curve simulation could be extremely time consuming. 2) The hardware data adjusts “model-to-hardware (MHC) scaling” that translates the simulated sensitivity curve to the hardware sensitivity curve. The second step is necessary to compensate for potential inconsistency of input power between simulation conditions and experiment environment. For the estimator, linear regression fitting is used.

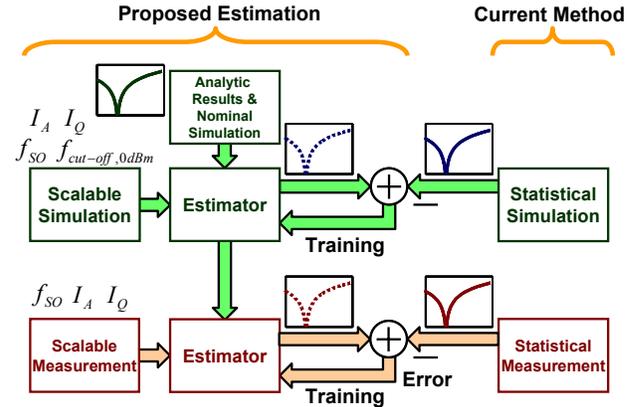


Fig. 5. Divider sensitivity estimation process flow with scalable simulations and measurements.

The correlation of f_{SO} and divider $f_{cut-off}$'s at 0dBm input signal power is shown in Fig. 6, using 500 Monte Carlo simulation points, at different V_{BIAS} 's. The $f_{cut-off}$'s were obtained by finding the minimum and maximum frequencies that divider operate with 0dBm input. The linear relationships confirm that the self-oscillation is an important parameter for sensitivity curve estimation. In

Fig. 7, a nominal sensitivity curve is shown as a green line, and $\pm 1-\sigma$ estimation errors at selected input powers are denoted as left and right triangles. The overall RMS error for all sample points is within 0.77GHz or 51% of standard deviation. In addition, there is a mismatch error from sample points to the whole nominal sensitivity curve after proper MHC-based scaling. This is a residual fitting error after scaling a nominal sensitivity curve to the best match sample points in terms of minimum mean-square error. The mismatch RMS difference is 2.4%, thus adding little to the overall estimation error. The information from V_{BIAS} points other than the $V_{BIAS}=0.6V$ further reduces RMS error from 4.4% to 0.5 % of mean. More detailed circuit nonlinear dynamics are captured when information other than $V_{BIAS}=0.6V$ are included.

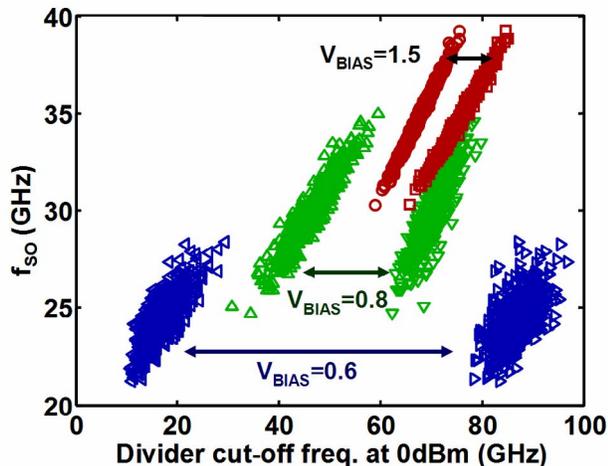


Fig. 6. Simulated divider f_{SO} versus the divider operation cut-off frequencies $f_{cut-off}$ at $V_{BIAS}=0.6, 0.8,$ and $1.5V$ for a 0dBm input.

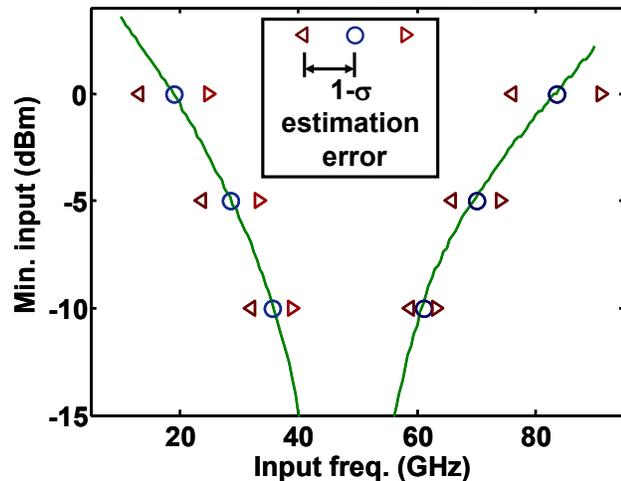


Fig. 7. Simulated RMS errors for divider sensitivity curve estimation. The estimation flow in Fig. 5 was used on the data in Fig. 6.

IV. DIVIDER MEASUREMENT AND ESTIMATION

Fig. 8 displays divider I_A vs. f_{SO} measurements from 76 chips in a 65nm SOI CMOS 300mm wafer. The f_{SO} variation at $V_{BIAS}=0.6V$ is seen as the 3-D wafer map. The variation for f_{SO} is 10.5% of the mean.

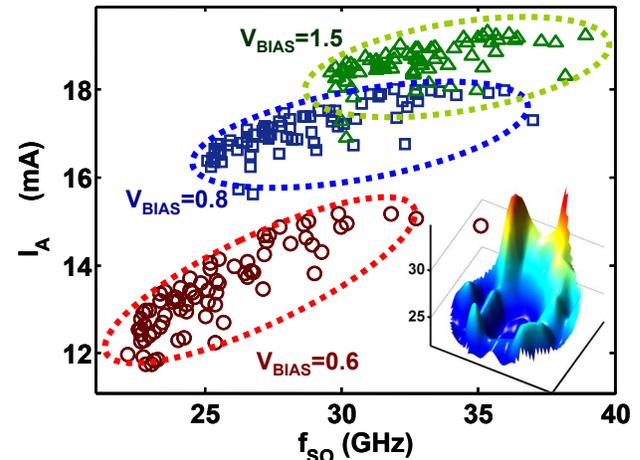


Fig. 8. CML static divider active current I_A and self-oscillation frequency f_{SO} measurements for $V_{BIAS}=0.6, 0.8,$ and $1.5V$ from a 300-mm 65nm SOI CMOS wafer.

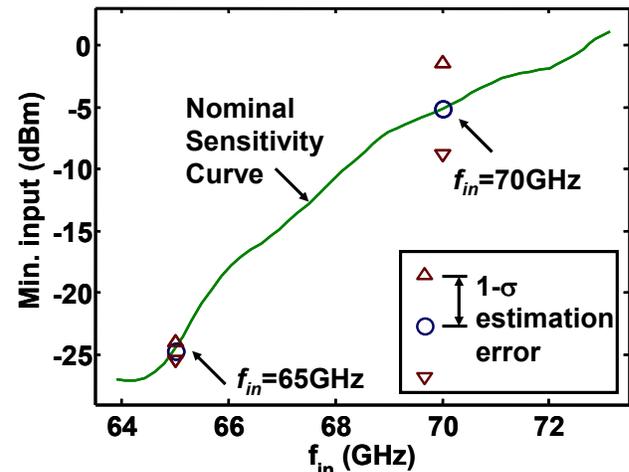


Fig. 9. Divider sensitivity statistical measurement and estimation error at $f_{in}=65GHz$ and $70GHz$. RMS error is 2.2dB or 55% of the standard deviation.

For the hardware data, only upper frequency region past f_{SO} is measured due to the W-band waveguide test set-up limits. Also the high-frequency divider operation range is more important for mmWave VCO and divider yield qualification. First, the nominal sensitivity curve was measured from 64GHz to 74GHz. For testing efficiency, input signal power is swept at fixed input frequencies of 65GHz and 70GHz. Due to the divider process variation, more than one input frequencies were needed for reliable

estimation. The more frequency points are sampled, the higher measurement accuracy is expected. Since the measurement is used for the validation of the proposed method, two separate frequencies were sufficient. Also, input power is swept instead of the frequency sweep in the simulation. The frequency sweep threshold measurement is more challenging than the input power sweep. It is because the phase shifters' optimal conditions at each frequency are compromised during the frequency sweep, and it aggravates the sensitivity in frequency sweep direction. As shown in Fig. 9, the overall RMS error is 2.2dB or 55% of standard deviation.

Currently divider performance characterization requires careful test setup and time-consuming procedure that are challenging to automate. A direct application of the presented sensitivity curve estimation is divider performance yield prediction inferred from statistical hardware data. Fig. 10 illustrates the divider yield as a function of input power and input frequency.

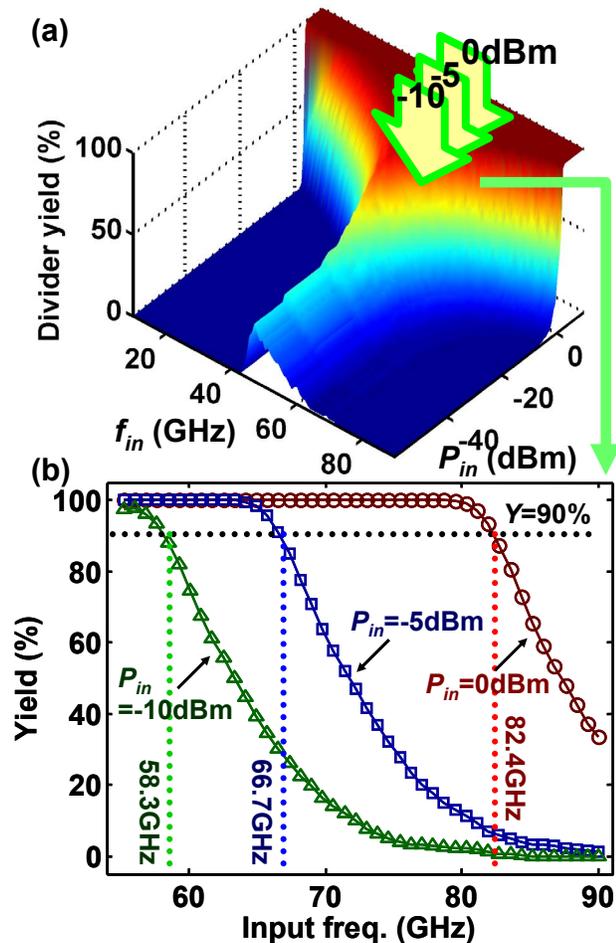


Fig. 10. CML static divider yield calculation based on the divider statistical measurements and estimation method.

Here, divider yield is calculated by the proposed method using the automated hardware measurements from 76 chips in the wafer. Therefore, it represents the actual manufacturability of the CML static divider within the accuracy of sensitivity curve estimation, thus allowing the accurate divider yield qualification. For a 0dBm input power to the divider, an 82.4GHz input signal is dividable with 90% yield. Also, the maximum dividable frequencies of 66.7GHz and 58.3GHz with 90% yield are obtained for -5 and -10dBm respectively. In the context of a PLL system where the output of VCO is connected into the input of a divider, this divider yield information is utilized for variation-aware VCO and divider design for mmWave PLL.

V. CONCLUSION

In this paper, an analytic equation for divider sensitivity curve is qualitatively formulated that relates the dividable bandwidth to the self-oscillation and DC parameters. A statistical methodology is then presented to estimate the divider's sensitivity curve based on self-oscillation frequency and DC measurements. Based on this analysis, an algorithm for sensitivity curve prediction is proposed and evaluated for the first time. The estimation RMS error for minimum input power is 2.2dB for hardware measurements. Divider performance yield is also predicted.

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