65nm SOI CMOS SoC Technology for Low-Power mmWave and RF Platform

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***Abstract*—An RF and mmWave platform developed in 65nm SOI CMOS technology is presented. The SOI FET performance in a wired cell is measured up to f_T=300GHz and 200GHz for NFET and PFET. Ring oscillator records 3.6psec minimum inverter stage delay. Back-end-of-line Vertical Native Capacitor (VNCAP) and on-chip inductor performances are reported. The performance scaling trends of mmWave PLL front-end components are presented.**

I. Introduction

The demands for higher bandwidth and high-performance SoC integration are driving CMOS mmWave and RF platform development. The CMOS technology scaling has improved not only the device density, but also the performance so far [1], [2]. The CMOS technology manifests SoC integration compatibility, technology road map, high-speed performance, and low manufacturing costs. But the up-front development costs, lack of high-power device and quality passive device, model accuracy, and aggravated process-induced variation that affects yield are limiting factors.

The silicon-on-insulator (SOI) CMOS technology has been a breakthrough for high-performance digital system implementation [3]. This paper introduces 65nm SOI technology as an analog mmWave and RF platform [4], [5]. The FETs (Section II), Back-End-Of-Line (BEOL) Vertical Native Capacitor (VNCAP) (Section III-A), and on-chip inductor (Section III-B) are presented. The performance scaling trends of mmWave PLL front-end circuits - complementary LC-VCO and CML static divider - are discussed (Section IV) as technology performance benchmark.

II. SOI FET

The SOI CMOS technology [2], [6] has buried-oxide (BOX) layer on the silicon substrate, and the body of the FET is partially doped and floating, as shown in Fig. 1. The BOX effectively cuts source and drain diffusion vertically, and it reduces diffusion parasitic capacitances, which is favorable to high-speed performance. For a fixed body potential device, a body-contact is formed with a T-shaped gate. It enables bulk-compatible circuits especially for analog design. The 65nm SOI technology features 35nm gate length and 10.5A nitrided film thickness. A dual stress nitride liner process enhances FET performances, and BEOL options are up to 10 1X, 2X, 4X, and 8X-metal layers.

The 65nm FET f_T performances are measured in Fig. 2 [7]. The DUT is a cell-based and wired FETs up to M2, and all contact resistances and near-range parasitic capacitances are included. The measurements are more practical for mmWave analog circuit design, since the immediate wiring parasitics impact more as technology scales down. Also the cell-based FET layout is defined by a rectangular area, and it makes layout, testing, and modeling highly scalable. The 2-port S-parameters are measured up to 50GHz, and open and short de-embedding is performed. The H21 gain is extrapolated to obtain f_T. As technology scales aggressively, the minimum gate-to-source and drain distances sacrifice device performance while achieving highest device density. The minimum spacing is called 1X pitch. By increasing the gate to contact pitch, gate-to-drain capacitance decreases, and the stress liner becomes more efficient. As a result, carrier mobility and device g_m increase, while the parasitic capacitance decreases. The pitch relaxing device option allows higher-speed performance for analog designs with an area trade-off. A 2X pitch FET f_T measurement with V_{gs} and V_{ds} sweeps is plotted in Fig. 2a, where the maximum f_T=307GHz is recorded. The

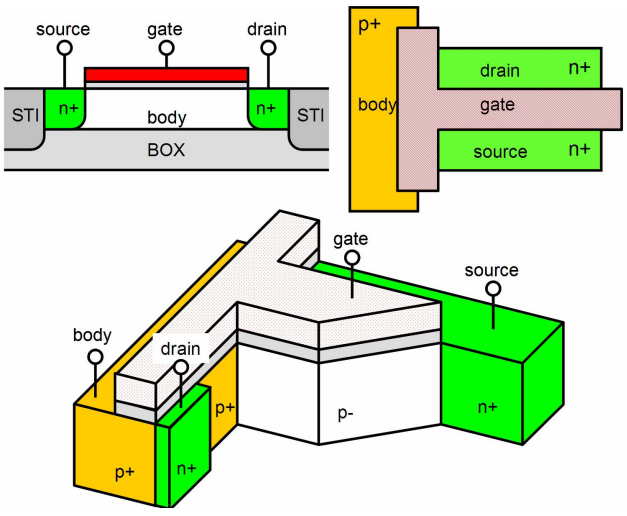

Fig. 1. SOI floating-body and body-contacted FET diagrams. The buried oxide layer effectively reduces diffusion volume and parasitic capacitances. A body contacted device is formed with a T-shaped gate and PN junction for analog design. Partially-depleted FETs are implemented in 65nm SOI CMOS.

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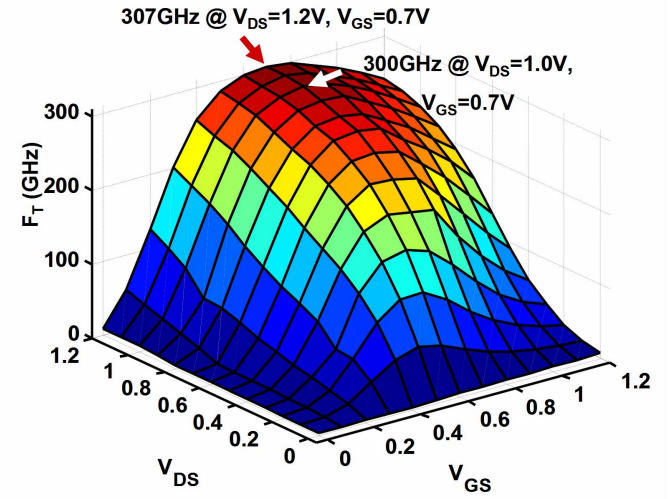

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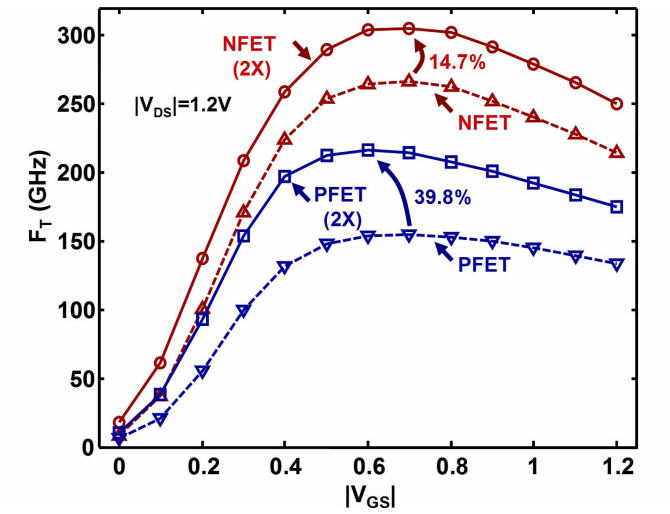

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Fig. 2. FET f_T performances in 65nm SOI CMOS. The pitch spacing between gate and contacts enhances FET high-speed performance by reducing parasitic capacitance and improving stress liner efficiency. (a) A 2X pitch NFET f_T measurements with V_{gs} and V_{ds} sweeps. S-parameters are measured up to 50GHz, and H21 line is extrapolated to obtain f_T. (b) NFET and PFET f_T performance improvements with 1X and 2X pitch. NFET and PFET f_T improve by 14.7% and 39.8%. The PFET f_T is greater than 200GHz.

f_T performances of 1X and 2X pitch devices are compared in Fig. 2b. The NFET and PFET improve by 14.7% and 39.8%. The 2X pitch PFET f_T is well beyond 200GHz.

Inverter-based 101-stage ring oscillators (ROs) are integrated with 1X and 2X pitch FETs [2]. The ROs have RF buffers, and the timed-domain waveform and oscillation phase noise are directly measured. A 300mm development wafer measurements are plotted in Fig. 3. The 2X pitch RO is about 16.9% faster than 1X minimum pitch RO. The phase noise of both ROs are also plotted in the figure. It was measured at 1MHz offset from the oscillation frequency, and the results are converted to a figure-of-merit that considers power consumption and oscillation frequency [8]. The 2X

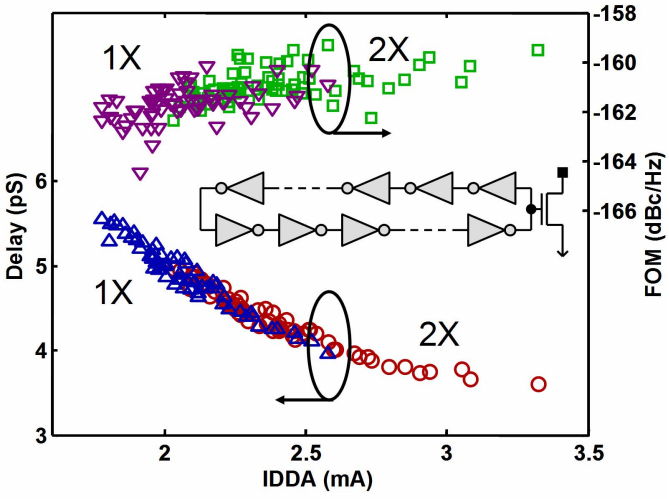


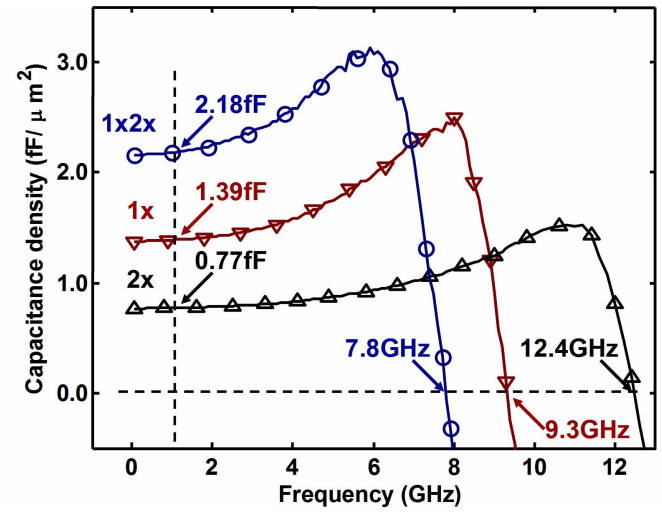
Fig. 3. Inverter-based 101-stage ring oscillator stage delay and phase noise measurements on a 300mm development wafer. The minimum gate delay record is 3.6psec. The 2X pitch RO is faster than 1X by 16.9%. The phase noise figures-of-merit are almost same in both ROs.

pitch device phase noise is similar to 1X device phase noise with slight deviation. The minimum inverter delay record is 3.6psec per stage.

III. SOI CMOS Passive Devices

A. Vertical Native Capacitor

RF SoC integration requires high-quality on-chip passive devices - inductor and capacitor. On-chip capacitor should have high capacitance density, linearity against voltage bias, low leakage current, and high Q-factor as specified in ITRS road map. The VNCAP is built with native BEOL metal layers, and it is manufactured within the standard masks and processes [9], [10]. The minimum metal feature size determines capacitance density, and it is expected that the capacitance density is scaled along the technology scaling. It has effective vertical-parallel plates for capacitance, and it is highly symmetric by nature. Three VNCAPs are fabricated in 65nm SOI with 1X (M1-M4), 2X (M5-M8), and 1X+2X layers. The 1X layer produces highest capacitance density, while the line resistance limits Q-factor. There are vias between layers, and vias contribute capacitance and reduce resistance. The via placements are arranged to maximize the BEOL processing yield. Each device is $100\mu m$ by $100\mu m$. Measurements are de-embedded with open and short. As plotted in Fig. 4a, the 1X+2X VNCAP shows 2.18fF/μm^2 at 1GHz. The 2X has lower capacitance density, but higher threshold frequency at 12.4GHz, where the VNCAP becomes an inductor. The Q-factors without de-embedding are plotted in Fig. 4b. The 2X VNCAP Q-factor is 90.1 at 1GHz. The de-embedding makes Q-factor high and it becomes singular in low-frequency region. The symmetry in RMS error is 0.09% when the capacitances from 2-port measurements are compared. The results show that the VNCAP density is scaled along the technology [10] with comparable Q-factors.



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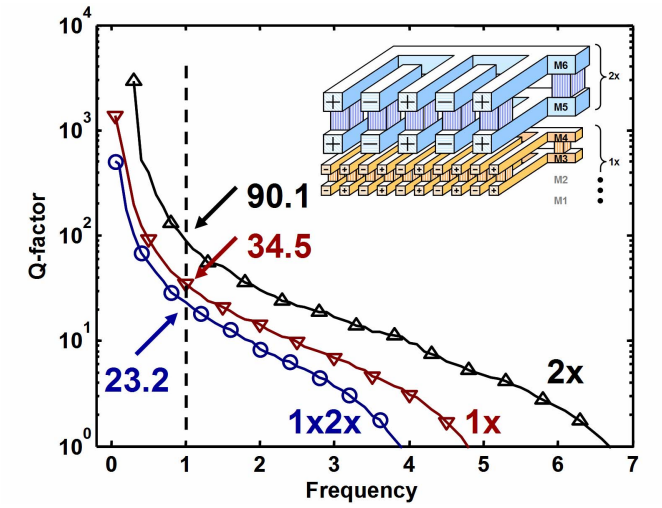

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Fig. 4. VNCAP diagram, density, and Q-factor. The VNCAP is built with various BEOL options. The highest density is available with the 1X layer, while higher Q-factor is obtained with thicker layer. Each VNCAP structure is $100\mu m$ by $100\mu m$. (a) VNCAP capacitance density. 1X+2X shows 2.18fF per μm^2, and 2X layer has higher threshold frequency at 12.4GHz. (b) VNCAP Q-factor plot before open and short de-embedding. High Q-factors make it difficult to de-embed precisely.

B. On-Chip Indictor

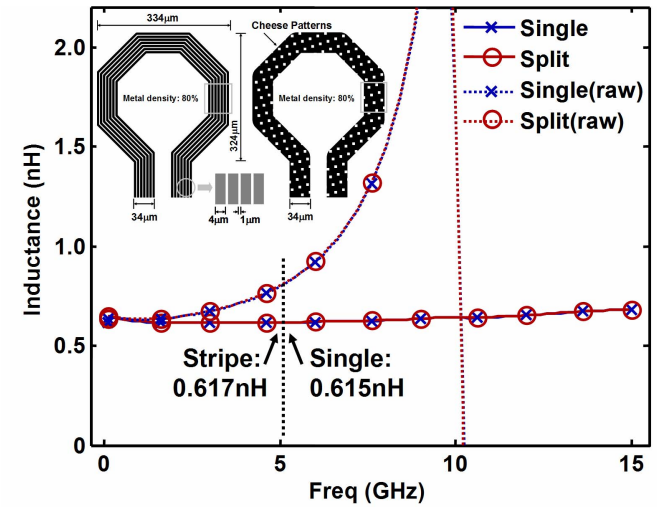
High-quality on-chip inductor integration is essential for RF system-on-chip manufacturing [11], [12]. In spite of the large real estate that an inductor occupies, the on-chip inductor performance, quality, and manufacturability are challenging in nanometer technologies. One of the critical factors that interfere with an on-chip inductor is BEOL metal density ratio as design rules. When an inductor is designed as a single wide metal line to reduce line resistance, it is subject to a post-layout "cheese" patterning and filling that enforce minimum and maximum metal density for improved manufacturability. A manufacturable striped inductor that actively engages the BEOL metal density rules is useful to enhance structure yield and model-to-hardware correlation (MHC). The striped inductor is manufactured as designed since it satisfies the technology's metal density rules. As a result, the striped inductor has better MHC. Also the sidewall area increases conductive surface, and it has lower RF resistance than a single-line, when the skin effect is considered. The striped and single-line inductor implementations in 65nm SOI technology are compared in Fig. 5. The inductors' 1-port s-parameters are measured from 50MHz to 25GHz. Calculated inductances are 0.617nH and 0.615nH at 5GHz as plotted in Fig. 5a. As long as the same layout dimensions are used, inductances of both inductors will be similar. The differences come out with Q-factor plots in Fig. 5b. The striped inductor Q is 13.5 and the single-line inductor Q is 13.2, about 2.2% Q-factor improvement. The Q-factor enhancement comes from reduced resistance. From 50MHz to 15GHz, the striped inductor has equal or lower resistance than the single-line inductor. The DC resistance of the single-line inductor is effectively increased by the patterning, since the patterning reduces the metal density to the technology requirement.

IV. PLL Front-End Circuit Performance Scaling

The FET high-speed performance does not always produce corresponding high-speed circuits. It is because the wiring parasitics in CMOS technology become more prevalent. The technology scaling introduces more capacitive coupling between conducting structures, and the line resistance increases accordingly. The discussed FET performance is based the wired FET cells, and the metrics are practical to use in the circuit design. Wiring parasitics are not normalized easily, and the real circuit performance serves as the benchmark metric.

CML static dividers are commonly used as technology performance benchmarks. A divider implemented in 65nm SOI performs up to 100GHz [13]. High-precision poly resistors are used to reduce parasitic loading to differential outputs. The master-slave latch-based divider utilizes VNCAPs for input signal AC coupling. It enables separate tail bias voltage control, and divider operation condition tuning. The divider performance has been scaled from 130nm to 65nm, as shown in Fig. 6 [13]–[15].

A complementary LC-VCO was implemented in 65nm SOI operating from 66.8GHz to 73.5GHz with 6.68GHz frequency tuning range [8]. The free-running VCO phase noise measurement is -106dBc/Hz at 10MHz offset, and the power consumption is 5.4mW at the core. The cross-coupled inverters take advantage of both NFET and PFET negative g_m pairs. The complementary design is favorable for low-power consumption and lower phase noise due to the symmetric topology. Considering β ratio between NFET and PFET, the oscillation frequency gets large penalty by the PFET use. The VCO oscillation frequency development in 130nm, 90nm, and 65nm SOI CMOS are plotted in Fig. 6 [8], [16], [17]. The frequency has been scaled over three nodes, though frequency tuning range, power, and phase noise should be also considered for a thorough comparison.



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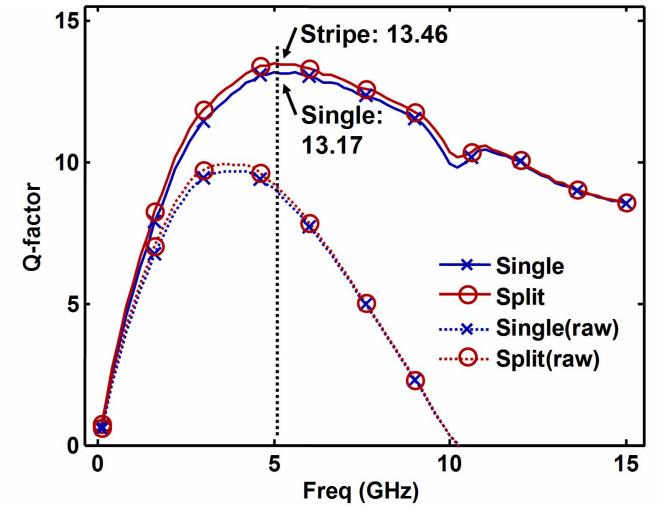

(b)

Fig. 5. On-chip inductor diagrams and measurements. The 1.2μm-thick top copper layer (M10) is used. The effect of BEOL CMP ratio enforcement and the striped inductor design are compared. Both inductors are affected by CMP fill patterns. The striped inductor is expected to have better model-to-hardware correlation and high-frequency performance. (a) Inductance measurement. (b) Q-factor measurement. The striped inductor has slightly higher Q-factor.

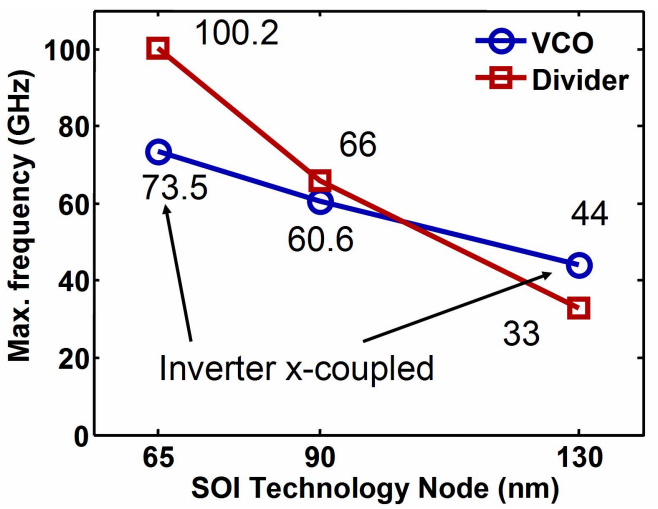

Fig. 6. SOI CMOS based LC-VCO and CML static divider performance scaling. The VCOs in 65nm and 130nm used complementary topology that employs both NFET and PFET negative g_m pairs. Considering PFET's lower DC and RF performances, the scaling has been effective in both FETs. The divider scaling has been stronger, and the VCO oscillation frequency is more affected by LC-tank and wiring parasitics.

V. Conclusion

An RF and mmWave platform in 65nm SOI CMOS technology was presented. The device and circuit performance scaling has been reported, and the platform enables high-performance mixed-signal SoC integration.

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