Performance and Yield Optimization of mm-Wave PLL Front-End in 65nm SOI CMOS

Daihyun Lim[1], Jonghae Kim[2], Jean-Olivier Plouchart[2], Daeik Kim[2],
Choongyeun Cho[2], and Duane S. Boning[1]
[1]MIT, Cambridge, MA, 02139, USA,
[2]IBM, Hopewell Junction, NY, 12533, USA

Abstract **— A combination of LC-VCO and 2:1 CML static frequency divider has been fabricated in 65nm SOI CMOS technology and operates at 70GHz. A cascoded buffer amplifier is used in VCO-to-divider connection to compensate for the power losses caused by interconnect parasitics, and inductive peaking is employed for bandwidth enhancement. The bias condition of the frequency divider has been tuned to find an optimal bias point in existence of VCO and frequency divider operating range variation. The inter-die variation of VCO and divider performance variations over a wafer and their correlation have been estimated.**

Index Terms **— Process variation, mm wave CMOS, VCO, frequency divider, inductive peaking.**

I. Introduction

Recently, progress in the performance of deeply scaled CMOS technology has resulted in successful implementation of CMOS radio systems operating in the millimeter wave band. Feature size scaling, mobility enhancement, and parasitic reduction in CMOS technology have continuously improved f_T, f_{max} and noise characteristic of CMOS devices and have enabled the design of CMOS millimeter wave systems [1]. However, scaling has also introduced critical performance variation issues due to the aggravated process variation in nano-scale devices and interconnects.

A *PLL front-end* consists of a VCO and 2:1 frequency divider as depicted in Fig. 1 (a). Since the PLL front-end operates at the highest frequency in the system, speed, power consumption, and noise characteristic must be considered carefully at the design stage. Furthermore, in an mm-wave band circuit, the tuning range of VCO is significantly narrowed by the reduced ratio between varactor to parasitic capacitance in scaled devices [2]. The operating range of the frequency divider is also limited since the input power has been reduced due to the loss in interconnects. Recently, 16.7% (3σ) variation in the self-oscillation frequency of dividers over a wafer in 65nm SOI technology has been reported [3]. Thus, the mismatch between the operating ranges of the VCO and frequency divider due to process variation can cause a serious yield problem in PLL integration.

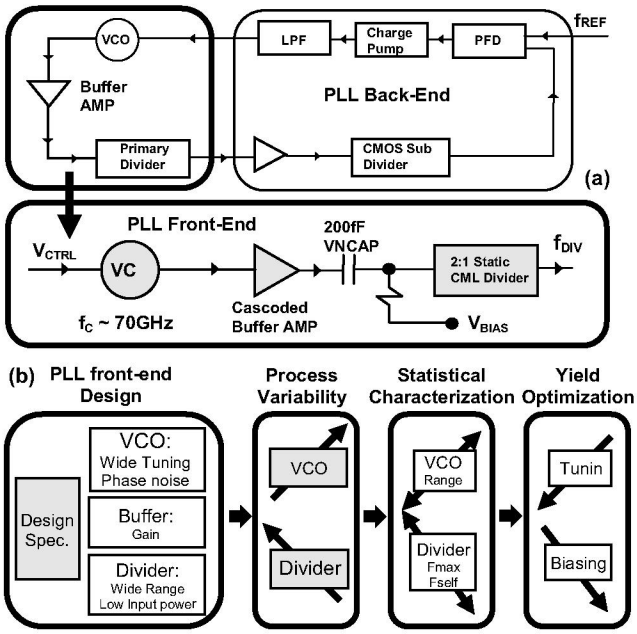

Fig. 1. Block diagram of a PLL and high-frequency building blocks.

The 70GHz PLL front-end, a combination of LC-VCO and 2:1 CML static frequency divider, has been implemented using IBM 65nm SOI CMOS in this work. As in Fig. 1 (b), the PLL front-end has been optimized following the design specifications of the VCO, frequency divider and buffer amplifier. The performance of the PLL front-end has been measured in a state-of-art mm-wave measurement setup. The statistical characteristics of the VCO tuning range and divider operating range variations have been estimated. Based on the measurement data, an optimal bias point for the highest yield of the PLL front-end has been investigated.

II. Design of mm-Wave VCO and Frequency Divider

A. Circuit Details

The schematic of the PLL front-end is shown in Fig. 2. Complementary LC-VCO design is employed with an

accumulation mode MOS varactor and C-shape inductor LC tank. The varactor gate length and inductor layout has been optimized for high-Q. One of the challenging issues in mm-wave CMOS VCO design is manufacturability; the wide tuning range is strongly needed to cover the desired frequency range in the presence of process variation. SOI technology has lower parasitic diffusion-to-substrate capacitance due to buried oxide layer isolation. The smaller FET parasitic capacitance provides large tunable range of the ratio between the varactor and parasitic capacitance, enabling a wide frequency tuning range of the VCO.

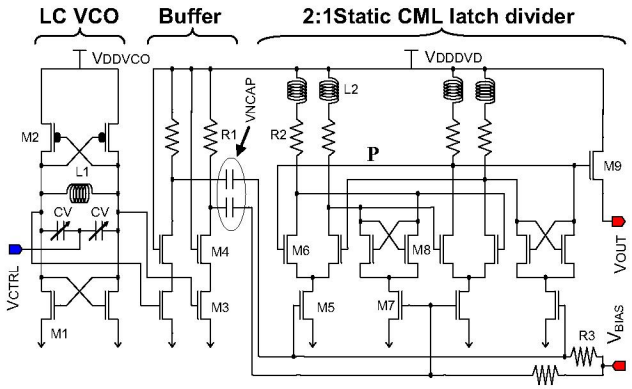

Fig. 2. Schematic of a 70GHz PLL front-end: an LC-VCO with a spiral inductor and accumulation mode MOS varactor and a 2:1 CML static frequency divider with inductive peaking.

The frequency divider uses CML master and slave latches with inductive peaking by four 300pH high-Q slab (metal plate) inductors for bandwidth enhancement. The bottom transistors (M5 and M7) are sized to 10μm to drive up to 10mA current. The size of the latch transistors (M8) is adjusted to 8μm to reduce capacitive loading at output nodes while satisfying the self-oscillation condition $g_{mL}R_L > 1$ with 230Ω poly-silicon resistor loads for high-speed operation [4]. Together, these circuit innovations enable exceptionally high speed operation at 70GHz of the PLL front-end circuit.

A cascoded amplifier with 100Ω poly resistor loads is employed as a buffer between the VCO and frequency divider. A 200fF state-of-the-art VNCAP [4] is used for the coupling of a VCO output signal to divider input. The buffer amplifier isolates the VCO output from large capacitive output loading including VNCAP parasitic (~20fF) and divider input capacitance (~10fF), and provides a gain of four for power loss compensation in interconnects. The on-chip AC coupling by the VNCAP enables V_{BIAS} to be controlled externally to change the bias currents in CML latches and tune the operating range of the frequency divider.

B. Simulation and Analysis

An input sensitivity curve accurately characterizes the frequency divider performance by showing the minimum required input voltage swing to lock the divider output at the desired frequency. Fig. 3 shows the simulated input sensitivity curves of the frequency divider at a fixed V_{BIAS} (=0.75V) with and without inductive peaking. The inductive peaking enhances the divider self-oscillation frequency by 2.75GHz, but when V_{min}>0.3V, the maximum operating frequency becomes similar to the case without the inductive peaking.

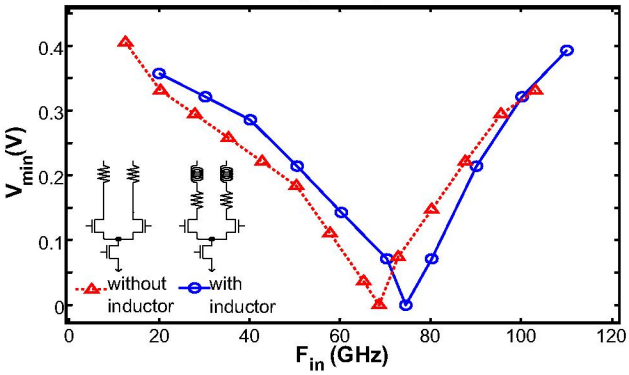

Fig.3. Simulated input sensitivity curves of the static CML frequency divider with and without inductive peaking.

For rail-to-rail square-wave inputs, the frequency divider can be analyzed as a simple digital flip-flop. However, for a power-limited input signal around twice of self-oscillation frequency, the operating mechanism of the frequency divider becomes similar to an injection locking oscillator. A large V_{BIAS} results in higher self-oscillation frequency while decreasing the operating frequency range of the frequency divider [5]. In Fig. 4, the simulated sensitivity curves of the frequency divider at various V_{BIAS} conditions shows that the divider operating range is highly sensitive to V_{BIAS}.

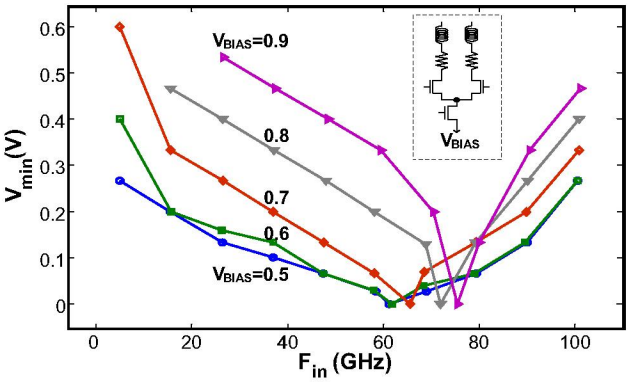

Fig. 4. Sensitivity curves of the frequency divider at various V_{BIAS} conditions showing the change of operating range.

C. Process Variation in the PLL Front-end Circuit

The self-oscillation frequency of the frequency divider is a function of bias current, load resistance, and parasitic capacitance at output nodes [3]. The bias current is highly sensitive to threshold voltage variation in bottom transistors (M5 and M7), and the threshold voltage change affects the self-oscillation frequency and operation range of the frequency divider similar to the V_{BIAS} changes in Fig. 4.

Fig. 5 illustrates how the change of V_{BIAS} affects the operation of the PLL front-end. From the inset figure of Fig. 5, the VCO operation is relatively robust compared to the divider against device skewing; the divider sensitivity variation is mainly considered in the PLL front-end. At $V_{BIAS,1}$, the divider sensitivity curve is well below the VCO output power over the VCO tuning range; the divider can operate in the full VCO tuning range. At $V_{BIAS,2}$, the VCO output power is partly below the sensitivity curve in the VCO tuning range, the divided frequency falls between the self-oscillation and correct divided frequencies in the failure region.

The V_{BIAS} can be increased more to set the self-oscillation frequency at the center of the VCO tuning range ($V_{BIAS,3}$), but it does not guarantee the stable operation over the full tuning range because of an extremely steepened sensitivity curve. On the other hand, higher V_{BIAS} results in larger output swing and provides larger gate over-drive of input devices to stabilize the divider performance against threshold voltage variation. Therefore, there exists an optimal V_{BIAS} condition considering the trade-offs in the PLL front-end design.

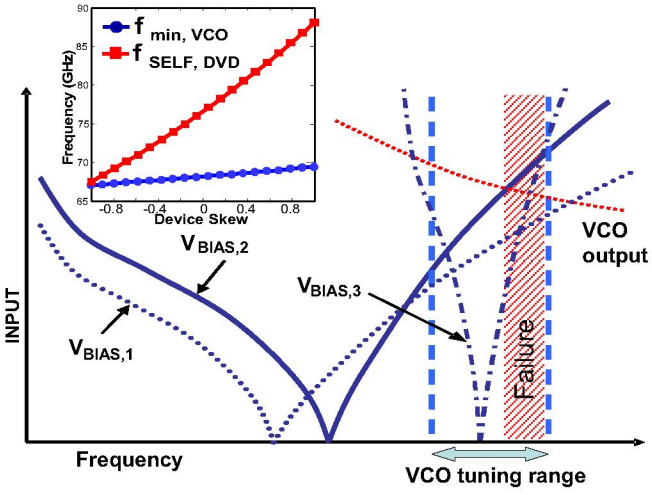

Fig. 5. Change of input sensitivity at different V_{BIAS} and coverage of VCO tuning range.

D. Implementation

Four types of the PLL front-end circuit are implemented in IBM 65nm SOI CMOS and the configuration of each type is summarized in Table 1. Type 1 and 2 utilize VCO_1 which has smaller PMOS/NMOS devices compared to VCO_2 in type 3 and 4 for smaller parasitic capacitance to achieve higher center frequency. There are two different types of divider layout: parasitic-aware layout and area-optimized layout. Wiring and device placement have been optimized in the area-optimized layout for smaller interconnect parasitics. Type 4 employs inductive peaking in addition to the area-optimized divider layout.

Table 1. PLL Front-end Configurations

	VCO	Frequency Divider
Type 1	VCO_1*	Parasitic-aware layout
Type 2	VCO_1	Area-optimized layout
Type 3	VCO_2**	Area-optimized layout
Type 4	VCO_2	Area-optimized layout + Inductive peaking

*VCO_1: 14um/28um NMOS/PMOS
**VCO_2: 17um/34um NMOS/PMOS

III. Measurement Results

A. VCO and Divider Variations

Fig. 6 shows the process variation in VCO tuning range and divider self-oscillation frequency over a wafer. These wafer-variation pattern is highly systematic; the cross correlation between different wafers is more than 90% on average. From the measurement of 65 dies (sites), type 3 and 4 circuits show 3σ of 3.52% in the minimum frequency variation over a wafer, which is similar to 3.54% of type 1 and 2. This shows that VCO tuning range variation is mainly caused by the variation in the MOS varactor which is identically sized in both VCO_1 and VCO_2.

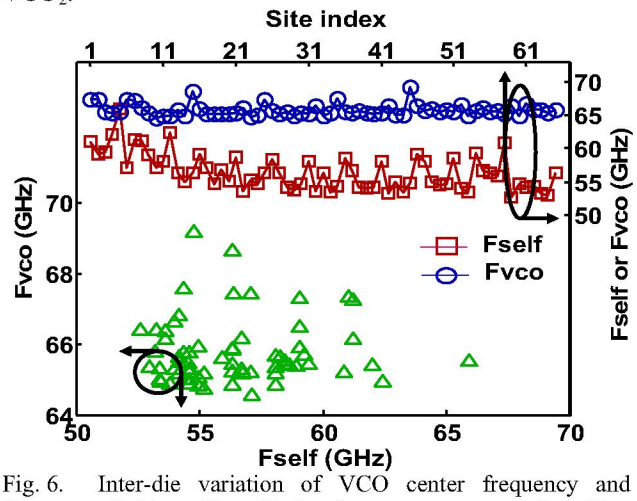

Fig. 6. Inter-die variation of VCO center frequency and frequency divider self-oscillation frequency over a wafer with a scattering diagram.

The spatial correlation between the two variations from the scattering diagram in Fig. 6 is not significant (ρ=0.17); VCO and frequency divider operating ranges do not track each other in the presence of significant inter-die variation. This result suggests an important concern in the PLL front-end design: the divider operating range must cover the VCO tuning ranges in both worst case combinations (fast VCO-slow divider and slow VCO-fast divider) to guarantee high manufacturing yield.

B. Yield Optimization

Fig. 7 shows the divider output frequency as V_{CTRL} changes from 0 to 1.2V for one of 76 tested dies. When V_{BIAS} is from 0.5V to 0.7V, the divider correctly generates correct divided frequency. At V_{BIAS}=0.8V, the divided frequency is down-shifted slightly since the sensitivity curve becomes close the VCO output power and the self-oscillation frequency starts to be mixed into the divider output. At V_{CTRL}=0.8V for the curve of V_{BIAS}=0.9V, the divider output departs from the desired output and instead converges to the divider self-oscillation frequency since the VCO output power is less than the minimum to lock the divider at the desired frequency. When V_{BIAS}=1.0 or 1.1V, the input power is well below the sensitivity curves, and the divider generates constant self-oscillation frequencies rather than divided VCO output frequencies.

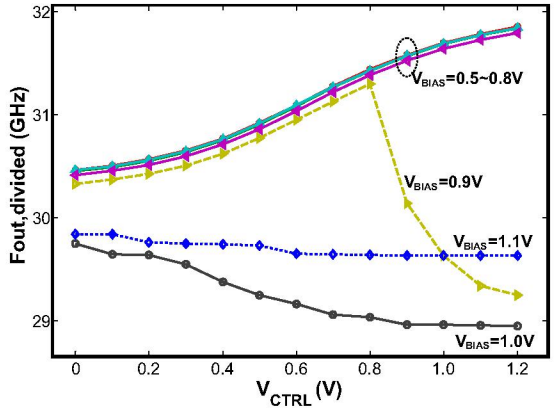

Fig. 7. Output frequency characteristic of the PLL front-end (type 4) over 0.0-1.2V V_{CTRL} sweep at various V_{BIAS} points for one die.

We define a sound PLL front-end circuit such that the divider operating range completely covers the tuning range of the VCO. Fig. 8 shows the yield of the four PLL front-end configurations when V_{BIAS} changes from 0.4 to 1.1V. The yield of type 1 and 2 is less than type 3 and 4 since the center frequency of VCO_1 is higher than VCO_2. The curves of type 3 and 4 explain that the impact of inductive peaking is negligible. The layout optimization does not show notable benefit in type 1 and 2. Overall, V_{BIAS} of 0.7V gives the optimum yield for all four configurations.

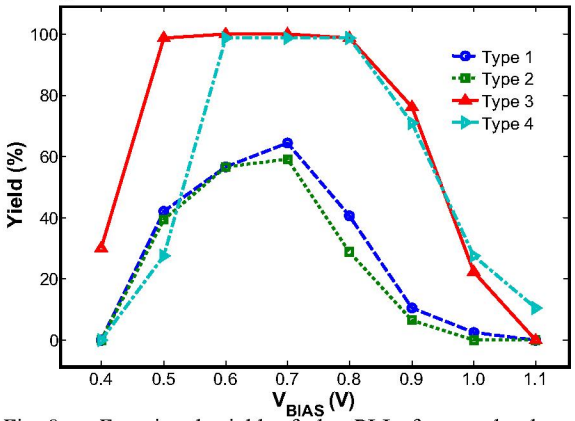

Fig. 8. Functional yield of the PLL front-end when V_{BIAS} changes from 0.4V to 1.1V.

V. Conclusion

A millimeter wave PLL front-end with LC-VCO and 2:1 CML static frequency divider has been implemented in 65nm SOI CMOS technology. The functionality of the VCO-divider combination has been tested in various bias conditions to find the optimal bias condition for highest circuit yield. The inter-die variation of the VCO and frequency divider has been measured and the spatial correlation in inter-die variation has been estimated.

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