A 1.2V 15.6mW 81GHz 2:1 Static CML Frequency Divider with a Band-Pass Load in a 90nm SOI CMOS Technology

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***Abstract* — A 2:1 static frequency divider using a band-pass load was fabricated in a digital 90nm SOI CMOS technology. The divider exhibits a maximum operating frequency of 81GHz at 1.2V, and a core power of 15.6mW. The divider can operate down to 0.5V at a maximum operating frequency of 75.6GHz with a core power of 2.75mW.**

***Index Terms* — frequency divider, CML, SOI, CMOS, low-power.**

I. Introduction

High-speed static 2:1 frequency divider circuits are required for many applications, from frequency synthesis in wireless communications, to quadrature signal generation and clock recovery in high-speed serial links. With a maximum operating frequency of more than 30GHz, the first static mmWave Current Mode Logic CMOS divider was reported at 130nm in 2003 [1]. CMOS performance scaling was demonstrated at 90 and 65nm with a reported maximum operating frequency of 66 and 90GHz respectively [2, 3]. As compared to other high-speed circuit functions, the static latch is a circuit with one of the highest fan-out. The static frequency divider is also limited by two times the delay of a single latch, therefore limiting the system's maximum frequency operation. Some new analog frequency divider topologies have been proposed to increase the maximum system operating frequency [4, 5]. In this paper we present the frequency, voltage and power performance improvement of a CML divider-by-two using a second order band-pass load.

II. Circuit Design and Optimization

Fig. 1 shows the block diagram of the 2:1 static band-pass frequency divider. It is based on CML master and slave latches connected in series. It can be shown that the cross connection between the output of the slave latch and the input of the master causes the clock frequency to be divided by two. All the latch data signals are differential. However, in order to save voltage headroom, the clock current sources were removed, and therefore the clock signals are pseudo differential [2]. The latches are biased by setting the gate voltage with an external bias-T. Some of the mismatch can be tuned out by adjusting the bias voltage of each clock gate separately. The output common drain buffer is also biased with an external bias-T. The buffer bias current can be monitored through the output bias-T. Therefore the output buffer and core divider power consumption can be monitored separately.

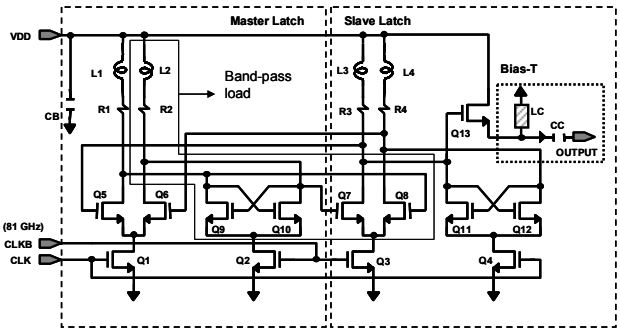

Fig. 1. Schematic of a static CML 2:1 frequency divider with inductive load.

Following circuit optimization, the widths of the clock and data differential-pair NFETs were designed to be 18.8μm and 15.12μm, respectively. Even though low-Vt NFETs are available in the technology, regular Vt NFETs were used for better transistor matching. A total of four 600pH slab inductor loads, each including a distributed 15 Ohms resistor, were used in the latches. In order to get the maximum circuit performance out of the technology the NFET layout was carefully optimized to achieve the best trade-off between F_t and F_{max} [6]. A first order analysis can show that F_t and F_{max} are monotonically increasing and decreasing functions, respectively, of the gate finger width. Therefore there is an optimum gate finger width resulting in the lowest CML switching delay. Also, very significant variations of performance can be observed as function of the FET and near FET wiring layout in nm CMOS technology. This is because in nm technologies, not all the electro-mechanical parameters scale

proportionally to the technology scaling factor, and also because of the stress engineering, the FET is not strictly an electrical device anymore, but it is now an electro-mechanical device. For an NFET the strain layer mobility enhancement increases the stress, therefore the mobility and F_t are a monotonically increasing function of the gate pitch (fig. 2). Also as shown in Fig. 2, the parasitic capacitors between the gate and the diffusion via contact decrease as a monotonically decreasing function of the gate pitch. These trends can be summarized by the following equations:

$$\begin{cases} F_t^{\uparrow}\left(W_f^{\uparrow}, \mu^{\uparrow}\left(pitch^{\uparrow}\right), C_{gsx}^{\downarrow}\left(pitch^{\uparrow}\right)\right) \\ F_{\max}^{\uparrow}\left(W_f^{\downarrow}, F_t^{\uparrow}, C_{gdx}^{\downarrow}\left(pitch^{\uparrow}\right)\right) \end{cases}$$

Where the geometric parameters are the gate pitch (pitch) and the gate finger width (W_f), μ is the electron mobility, the source and drain extrinsic parameters are C_{gsx} and G_{gdx}.

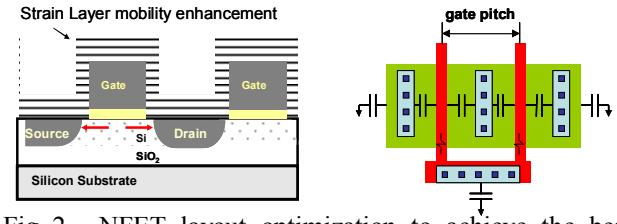

Fig. 2. NFET layout optimization to achieve the best trade-off between F_t and F_{max}.

III. FABRICATION

The circuit is fabricated in a 90nm IBM SOI CMOS microprocessor technology with 8 copper metal layers [7]. The manufactured NMOS transistors have cut off frequencies of 240 GHz and more than 200 GHz for the current gain (F_T) and maximum available power gain (F_{max}) respectively [7].

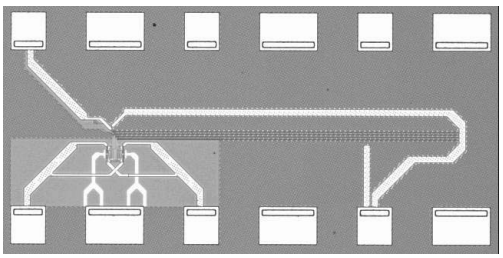

Fig. 3. Divider chip microphotography (dimension: 0.9mm x 0.5mm).

The technology offers a wide variety of high-Q passives such as inductors (Peak Q>20), accumulation varactors, and interdigitated back-end linear capacitors, without requiring any added technology steps. The technology offers polysilicon resistors as well. The chip size is 0.9x0.5mm² including the three mmWave input and output pads as well as the four slabs inductors. The dividers were fabricated on an SOI Substrate with resistivity of 12 Ohm.cm.

IV. ON-WAFER MMWAVE TESTSET UP

The test setup used for the divider characterization is shown in Fig. 4. One of the difficulties was to generate a differential clock beyond 60GHz, as well as providing a bias for the in phase and out of phase clock signals. As shown in Fig. 4 the signal generator provides a signal of more than 10dBm that is then multiplied in frequency by six. The output of the multiplier is a WR10 wave guide. The signal is amplified by a waveguide amplifier and the amplitude is controlled by a mechanical variable attenuator. Two waveguide phase shifters adjust the phases of both signals. In order to provide the bias, a diplexer was used with a WR10 waveguide input for the mmWave clock signal, a 1.85mm input connector for the bias and a 1mm coaxial cable output. A 1.1dBm signal was measured with a power meter at 81GHz at the 1mm cable output. All measurements were performed directly on wafer with 110GHz wedge probes. The output power is monitored with a 50GHz spectrum analyzer with phase noise measurement capability.

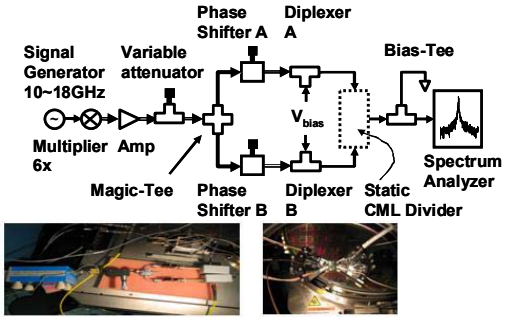

Fig. 4. On-wafer mmWave measurement set-up.

V. MEASUREMENT RESULTS

Fig. 5 shows the maximum operating frequency and core divider power consumption as function of VDD. The CML latch can operate down to 0.5V VDD, and can be clocked at a maximum operating frequency of 75.6GHz. To the authors' knowledge this is the highest speed and lowest voltage reported for a CML latch. At 0.5V VDD, the core divider current is 5.5mA, the core power consumption is 2.75mW and the buffer current is 0.5mA.

The measured output power is -34dBm at 75.6GHz. When the VDD voltage supply is increased the maximum operating frequency increases, up to 81GHz at 1.2V, with a core divider current and power of 13mA and 15.6mW respectively. The buffer amplifier current is 8.9mA and the measured output power is -20.2dBm at 40.5GHz output. Beyond 1.2V the maximum operating frequency does not improve.

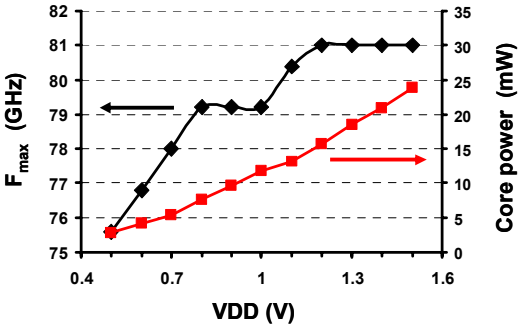

Fig. 5. Maximum operating frequency (Fmax) and core power versus VDD.

Fig. 6 shows the divider 50GHz broadband output spectrum at 1.2V VDD voltage supply, with a 40.5GHz output signal when a 81GHz input signal is applied.

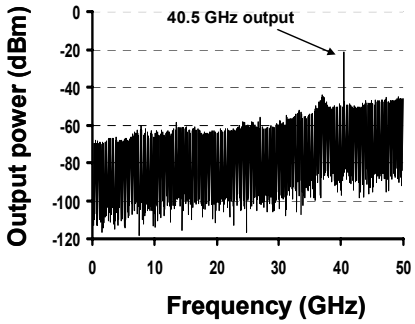

Fig. 6. Output spectrum with 81GHz clock input at 1.2V VDD.

Fig. 7 shows the divider input sensitivity as a function of the input divider frequency measured with the WR10 system at 1.2V VDD. The sensitivity curve has a minimum corresponding to the self-oscillation of the CML divider. When no signal is applied at the input the divider behaves like a ring oscillator, with an output self-oscillation frequency of 34.67GHz (F_{oso}). Referred to the input the self-oscillation frequency is 69.3GHz (F_{iso}), and corresponds to the sensitivity curve minimum. The maximum operating frequency of 81GHz is limited by the maximum available power of 1dBm at the output of the 1mm coaxial cable. Also, the input clock signal is further attenuated by 3dB based on the estimated 1.5dB loss in the 1mm coplanar probe and 1.5dB loss in the input chip pad. The minimum operating frequency is 64.8GHz, and is limited by the WR10 test set-up cut-off frequency.

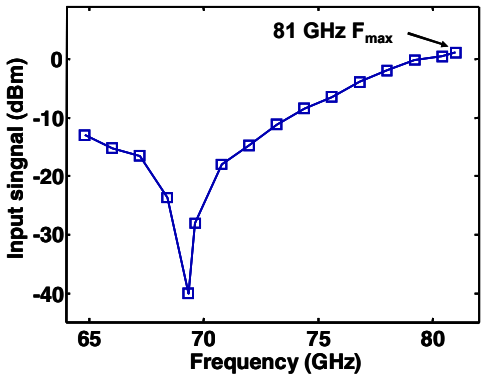

Fig. 7. Divider input sensitivity as a function of input frequency measured at 1.2V VDD.

Fig. 8 shows the output phase noise measured at 40.5GHz after division of the 81GHz input signal. A -98.6dBc/Hz is achieved at 100KHz offset of the 40.5GHz carrier. At 1MHz offset frequency the phase noise is -112.6dBc/Hz. This is comparable to the SiGe CML divider phase noise reported in [9] with a -96.4dBc/Hz measured at 100KHz offset of the 50GHz carrier. However the measured noise floor is -112.6dbc/Hz for this work versus -106dBc/Hz for the SiGe design reported in [9]. This difference could be attributed to the input source signal, the latch, or the buffer noise floor performance. It is worth to note that despite higher corner flicker noise frequency for CMOS than for SiGe bipolar technologies, this work shows phase noise performance as good as or better than state of the art SiGe noise performance [9].

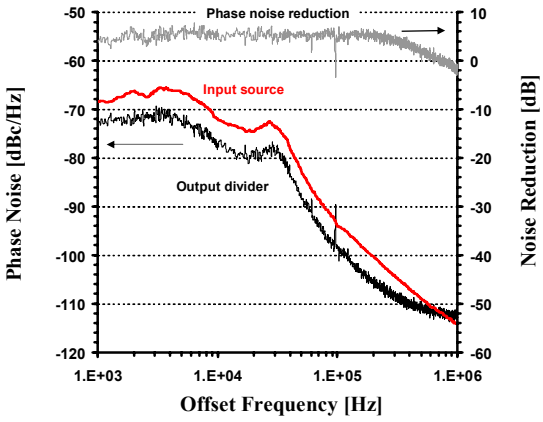

Fig. 8. Output divider phase noise measure for a 81GHz input signal at 1.2V VDD.

VI. STATE OF THE ART COMPARISON

A summary of state of the art frequency dividers is shown in table I. This work increases by 23% the 90nm CMOS state of the art for maximum CML latch operating frequency [2]. Owing to the slab inductor load the voltage supply can be decrease from 1.8 to 1.2V VDD, and the core power is reduced by 80%. The draw back of the slab inductor load is a significant area penalty. As shown in Table I, we also report a divider core power in this work more than 83 to 97% lower than state of the art compound semi-conductor, for a self-oscillation frequency only 27% lower [8]. The self-oscillation frequency is a more accurate way of comparing divider speed, since the maximum operating frequency depends of how much power can be provided at the circuit input transistor. At 0.5V VDD, the latch gain is not high enough for the divider to self-oscillate, but because the input clock FET operates in class AB, once the mmWave power is turned on, the current bias increases and the latch gain is high enough for the divider to operate properly. One way to compare the latch efficiency is to compute the switching energy as defined by:

$$Energy = \frac{Power}{8 \cdot F_{\max}} \quad (1)$$

This assumes two gate delays per flip-flop and an equivalent complexity of four logic gates. The effective number of logic gates is only important in comparing divider results to ring oscillators. With a record switching energy of 24 and 4.6fJ, we demonstrate the advantages of the band-pass load and lower FET threshold voltage as compared to the HBT, in enabling low-voltage operation.

TABLE I
SUMMARY OF STATE OF THE ART CML DIVIDERS

Fosc [GHz]	Fmax [GHz]	Power [mW]	VDD [V]	Energy [fJ]	Technology
48	66	80	1.8	152	90nm CMOS [2]
95	143.6	90	N.A.	78	InP HBT [8]
77	100	122	3.3	153	SiGe HBT [9]
69.4	81	15.6	1.2	24	This work, 90nm CMOS
N.A.	75	2.75	0.5	4.6	This work, 90nm CMOS

VII. CONCLUSION

A static CML divider with a band-pass load was designed in a 90nm SOI CMOS technology. The divider exhibits an increase of 23% in maximum operating frequency at 33% lower voltage supply and 80% reduction in power as compared to static CML divider with a low-pass load. A switching energy of 24fJ is measured at the maximum operating frequency of 81GHz.

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REFERENCES

[1] Jean-Olivier Plouchart, Jonghae Kim, Hector Recoules, Noah Zamdmer, Yue Tan, Melanie Sherony, Asit Ray, and Lawrence Wagner "A 33 GHz 2:1 Static Frequency Divider in 0.12-μm SOI CMOS Operable at 2.7mW," *IEEE RFIC 2003 Dig.,* pp. 329 - 332, June 2003.

[2] Jean-Olivier Plouchart, Jonghae Kim, Victor Karam, Robert Trzcinski, and Jeff Gross, "Performance Variations of a 66GHz Static CML Divider in a 90nm CMOS," *IEEE ISSCC 2006 Dig.*, pp. 526-527, Feb. 2006.

[3] Daihyun Lim, Jonghae Kim, Jean-Olivier Plouchart, Robert Trzcinski, and Duane Boning, "Performance Variability of a 90GHz CML Frequency Divider in a 65nm SOI CMOS," *IEEE ISSCC 2007 Dig.*, pp. 542-543, Feb. 2007.

[4] G. von Buren, C. Kromer, F. Ellinger, A. Huber, M. Schmatz, H. Jackel, "A Combined Dynamic and Static Frequency Divider for a 40GHz PLL in 80nm CMOS," *IEEE ISSCC 2006 Dig.*, pp. 2462-2471, Feb. 2006.

[5] Behzad Razavi, "Heterodyne Phase Locking: A Technique for High-Frequency Division," *IEEE ISSCC 2007 Dig.*, pp. 428-429, Feb. 2007.

[6] J.-O. Plouchart, "SOI 90-nm Ring Oscillator Sub-ps Model-Hardware Correlation and Parasitic-aware Optimization to 1.94-ps Switching Delay," 2005 International Electron Devices Meeting, Dec. 2005

[7] J.-O. Plouchart, N. Zamdmer, J. Kim, R. Trzcinski, S. Narasimha, M. Khare, L.F. Wagner, S.L. Sweeney, S. Chaloux, "A 243-GHz Ft and 208-GHz Fmax, 90-nm SOI CMOS SoC Technology With Low-Power mmWave Digital and RF Circuit Capability," *IEEE Transactions on Electron Devices*, Volume 52, Issue 7, pp. 1370 – 1375, July 2005.

[8] D. A. Hitko, et al. "A Low Power (45mW/Latch) Static 150 GHz CML Divider," *IEEE CSICS 2004 Dig.*, pp. 167–170.

[9] E. Laskin, S. T. Nicolson, P. Chevalier, A. Chantre, B. Sautreuil, S. P. Voinigescu, "Low-Power, Low-Phase Noise SiGe HBT Static Frequency Divider Topologies up to 100 GHz," *IEEE BCTM 2006 Dig.*, pp. 526-527, Feb. 2006.