SOI CMOS Technology with 360GHz f_T NFET, 260GHz f_T PFET, and Record Circuit Performance for Millimeter-Wave Digital and Analog System-on-Chip Applications

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Abstract

We present record-performance RF devices and circuits for an SOI CMOS technology, at 35nm L_{poly}. Critical RF/analog figure of merits in FET such as current gain cut-off frequency (f_T), 1/f noise, and high-frequency noise figure at various bias and temperature conditions are measured and modeled to enable high-performance circuit design. Measurement results show peak f_T's of 340GHz and 240GHz for 35nm L_{poly} NFET and PFET, respectively. At sub-35nm L_{poly}, 360GHz f_T NFET and 260GHz f_T PFET are demonstrated. High-Q, high-density vertical native capacitors (VNCAPs) and on-chip inductors are integrated. RF-operable ring oscillator (RFRO) demonstrates a 3.58psec delay and a SSB phase noise of -107dBc/Hz at 1MHz offset. LC-tank VCO operates at 70GHz with 9.5% tuning range. The maximum operating frequency of a static CML divider is 93GHz while dissipating 52.4mW.

Device Performances

The 65-nm SOI CMOS technology features 35nm L_{poly}, dual-stress nitride liners, and eSiGe-enhanced PFET [1, 2]. The high-speed, low-noise characteristics of SOI CMOS technology [3] not only enhance high-performance microprocessor circuits, but also enable digital and RF/analog system-on-chip (SoC) applications [4]. To enable circuit design, it is critical to characterize and optimize RF/analog properties. Fig. 2 shows the measured current gain cutoff frequency (f_T) and transconductance (g_m) vs. V_{GS} at V_{DS} of +1V for NFET at 27nm L_{poly}. Peak f_T's of 330GHz for fully-wired FET, 360GHz for intrinsic FET where circuit-level wiring parasitics are de-embedded, and peak g_m of 1.61mS/μm are measured at V_{GS} of 0.6V, as shown in Fig. 2. Figs. 3 and 4 show V_{GS} dependence of f_T and g_m in 35nm L_{poly} NFET/PFET at -40, 25, 125°C. While record high-speed performances (peak f_T's of 370GHz and 260GHz, peak g_m's of 1.62mS/μm and 1.04mS/μm for NFET and PFET) can be achieved at low temperature, RF characterization and modeling at high temperature enable worst-case circuit design. Bias (V_{GS}) dependence of f_T and g_m shown in Figs. 2, 3, and 4 demonstrates that the channel and threshold voltage are well controlled. Fig. 5 shows CMOS RF performance (f_T) scalability with L_{poly}. At sub-35nm L_{poly}, peak f_T's of 360GHz and 260GHz for NFET and PFET are measured, as shown in Fig. 5. The f_T's for NFET and PFET together are the best ever reported in a 65-nm CMOS technology [3, 5]. Relaxed pitch layout employed in this technology improves RF performance in comparison to regular pitch layout [3]. Also shown in Fig. 5 is that advanced 65-nm SOI technology [1] achieves the same f_T at longer L_{poly} in comparison to base 65-nm SOI [2] and bulk CMOS [5] technologies, thus demonstrating more aggressive RF performance scaling capability.

Fig. 6 shows the measured NF_{min} vs. frequency in NFET and PFET with floating-body and body-contacted layout. NF_{min} is measured on wafer without de-embedding thermal noise contribution from pad parasitics; therefore, intrinsic FET noise performance should be better. Note that PFET demonstrates low-noise characteristics comparable to those of NFET and that body-contacted FET compares well with floating-body FET in terms of high-frequency noise performance. Fig. 6 also shows that the high-frequency noise performance can be optimized by narrower width, multiple finger layout to minimize the thermal noise contribution from poly resistance [3]. Low-frequency 1/f noise is important in RF/analog circuit design (e.g., RF oscillator, PLL). Fig. 7 shows the measured low-frequency noise characteristics at various bias conditions in floating-body NFET. For floating-body SOI FET, an excess low-frequency noise with Lorentzian spectrum in addition to 1/f noise results from diode current-induced shot noise, amplified by floating-body effect, which is more pronounced at lower V_{DS}, as shown in Fig. 7.

Passives are key to the integration of high-speed digital and RF/analog circuits. VNCAP uses vertically stacked comb-shape metal lines and vias to build capacitance as depicted in Fig. 1 (H). It does not require additional masks while metal-insulator-metal (MIM) capacitor does, and it is highly manufacturable since it uses standard metallization. With native back-end of the line (BEOL) metal layers and via structures as shown in Fig. 1 (B), maximum capacitance density of 1.72fF/μm² and Q of 20 at 1GHz can be achieved, as shown in Fig. 8. The capacitor density is linearly scalable due to four different VNCAPs with different metal layer and via options. On-chip inductors are readily integrated with 1.6μm-thick upper copper layers. An octagonal single-turn and single-layer RF inductor layout with 34μm-wide metal line on area of 334×380μm^2 is shown in Fig. 1 (G), and Fig. 9 shows the measured inductance and Q-factor vs. frequency.

Circuit Performances

Two types of RF-operable ring oscillators (RFRO and $RFRO_W$) are designed with regular and relaxed pitch layout FETs. While typical ring oscillator is measured indirectly with frequency divider, RFRO is measured directly at high frequency with RF buffer amplifier at the output, as shown in Fig. 1 (J). The designed 101-stage $RFRO_W$ performs up to 1.3816GHz oscillation at 2μW power dissipation. This oscillation frequency is translated to the delay of 3.58psec per gate. Fig. 10 shows ring oscillators' delay and SSB phase noise performance vs. dynamic current (I_{DDA}) measured on a 300mm full wafer. The $RFRO_W$ is 12% faster than RFRO while the SSB phase noise performance is similar between $RFRO_W$ and RFRO, as shown in Fig. 11. The LC-tank VCO operates over 70GHz at 5mW power dissipation, and the frequency tuning range (FTR) is 9.5%, overcoming the CMOS process variations [6], as shown in Fig. 12. The CML dividers' self oscillation frequencies are experimented with two different types of CML dividers (divider type (A) for resistor load only and divider type (B) for inductive peaking load). The self oscillation frequency ($F_{SELF-OSC}$) can be projected into the divider sensitivity (Sensitivity = $(2+\alpha) \cdot F_{SELF-OSC}$) without the sensitivity experiment directly, and Fig. 13 shows the sensitivity measurement results for two different types of dividers.

Conclusion

A 65-nm SOI CMOS technology demonstrates high performance digital and RF/analog capabilities with 360GHz f_T NFET with sub-1.3dB NF_{min} at 18GHz, 260GHz f_T PFET, and high-Q, high-density VNCAP and inductor. Three core circuits: RF ring oscillator, LC-tank VCO, and CML divider, demonstrate record high-speed performances, and therefore can be used as technology benchmark circuit and evaluation guide for digital and RF circuits for real system-on-chip applications.

References

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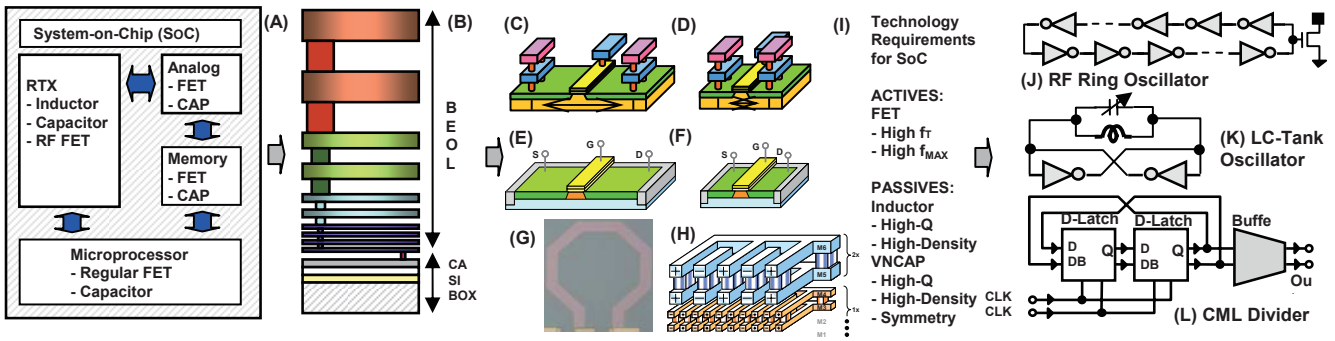

Fig. 1. (A) System-on-Chip device component diagram with RF, analog, memory, and digital processing cores, (B) technology cross-section, (C) fully-wired, relaxed pitch FET, (D) fully-wired, regular pitch FET, (E) intrinsic, relaxed pitch FET where wiring parasitics are de-embedded, (F) intrinsic, regular pitch FET, (G) C-shape inductor (W=35μm, L= 1000μm), (H) 3-D VNCAP, (I) Technology requirements for SoC, (J) RF ring oscillator, (K) LC-tank oscillator, (L) CML divider.

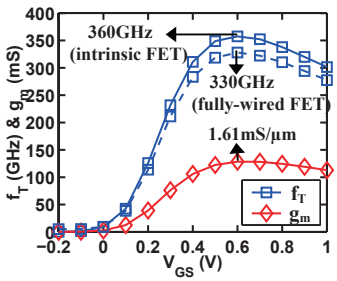

Fig. 2. Measured f_T & g_m vs. V_{GS} at V_{DS} = 1V for 27nm L_{poly}, 80μm width NFET.

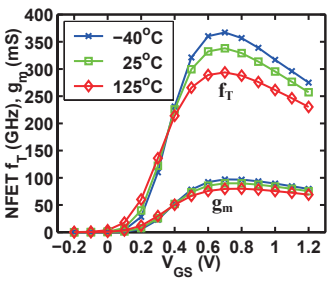

Fig. 3. Measured f_T (intrinsic) & g_m vs. V_{GS} at V_{DS} = 1V at -40, 25, 125 °C for 35nm L_{poly}, 60μm width NFET.

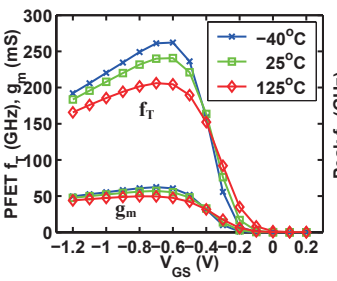

Fig. 4. Measured f_T (intrinsic) & g_m vs. V_{GS} at V_{DS} = 1V at -40, 25, 125 °C for 35nm L_{poly}, 60μm width PFET.

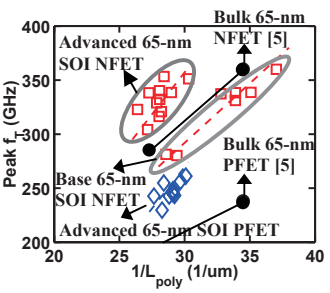

Fig. 5. Measured RF CMOS peak f_T (intrinsic) vs. $1/L_{poly}$.

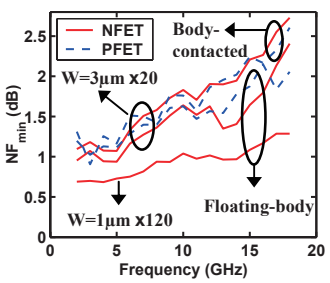

Fig. 6. Measured NF_{min} vs. frequency for 35nm L_{poly} NFET at V_{GS} = 0.5V, V_{DS} = 1V, for PFET at V_{GS}= -0.4V, V_{DS} = -1V

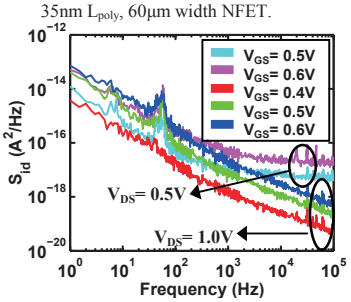

Fig. 7. Measured low-frequency noise for 35nm L_{poly} NFET (floating-body).

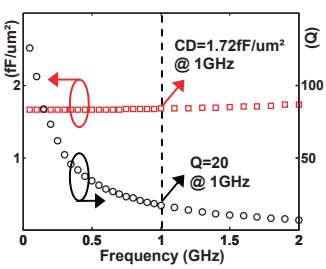

Fig. 8. VNCAP: Measured capacitance density and Q-factor vs. frequency.

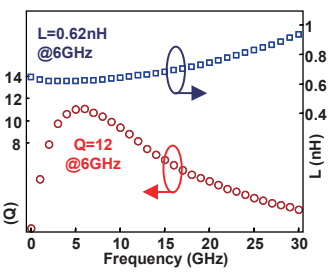

Fig. 9. On-chip inductor: Measured inductance and Q-factor vs. frequency.

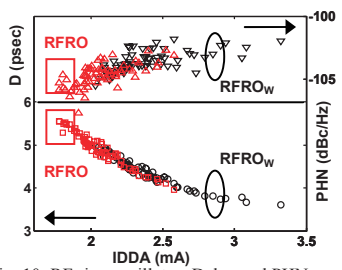

Fig. 10. RF ring oscillator: Delay and PHN vs. IDDA (D: Delay, PHN: SSB phase noise).

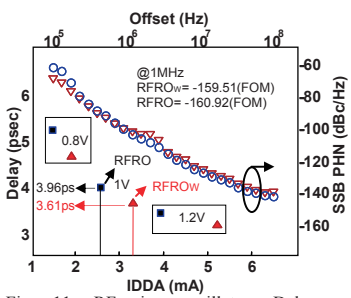

Fig. 11. RF ring oscillator: Delay performance versus power supply and FOM for two RF ring oscillators.

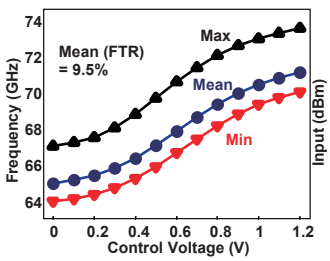

Fig. 12. LC-VCO: Highest and lowest tuning frequencies versus site (60 sites on a 300mm wafer).

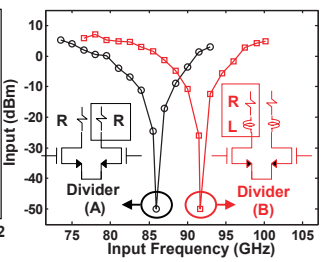

Fig. 13. CML divider: Dividers' sensitivity measurement for input power level (Divider (B) > Divider (A)).

Table 1. RF perfromance Summary for 65-nm SOI CMOS Technology

No.	*(Active Devices)*	Size (L_{poly} x width)			Intrinsic FET f_T (fully-wired FET f_T)			g_m	NF_{min} (measured on wafer)	
1	NFETw @ V_{DS}= 1V	0.035μm x 60μm			340GHz (315GHz)			1.50mS/μm	1.64dB @15GHz	
2	PFETw @ V_{DS}=-1V	0.035μm x 60μm			240GHz (225 GHz)			0.96mS/μm	1.87dB @15GHz	
----	*(Passive Devices)*	Tech.	Size	Inductance	Densities (Inductance/area)			Quality Factor	Metal Stack	
3	INDUCTOR	B.E.O.L	334x380μm²	0.62nH	4.756fH/ μm²			12@6GHz	M10 (1 metal layer)	
----	*(Passive Devices)*	Tech.	Size	Capacitance	Densities (Capacitance/area)			Quality Factor	Metal Stack	
4	VNCAP	B.E.O.L	100x100μm²	17.2pF	1.92fF/μm²			20@1GHz	M1-M6 (6 metal layers)	
----	*(Tech Benchmarking)*	Used Active Devices		Size (width)	IDDA	PDISS	Delay	Oscillation Frequency	Delay-Per-Stage	
5A	RO_regular_pitch	NFET / PFET		3μm / 6μm	2.0E-6	2μW	5E-12	Mean = 1.1816GHz	5 psec	
5B	RO_relaxed_pitch	NFETw / PFETw		3μm / 6μm	2.5E-6	2.5μW	4E-12	Mean = 1.3816GHz	4 psec	
----	*(RF Circuit)*	Used Devices			F_{OSC}	Mean FTR	Pdiss	SSB Phase Noise (70GHz)	FOM	FOM_T
6	V-band VCO	NFETw, PFETw, Inductor			> 70GHz	9.5%	5mW	-106dBc/Hz@10MHz	-166.80	-166.36
----	*(High Speed)*	Used Devices			FSELF-OSC		Max. Dividable Freq	Operating Frequency		
7	CML Divider (B)	NFETw, Resistor, Inductor, VNCAP			31GHZ		~100GHz	FOP = FSELF·(2 + α) = 93GHz with α=1		

(Note: NFETw: relaxed pitch NFET, PFETw: relaxed pitch PFET, FTR: frequency tuning range, FOP: operable frequency, FOM=SSB phase noise (Δω)-20log(ωo/Δω)+10log(Pdiss/1mW), FOM_T = FOM -20log(FTR/10), $F_{SELF-OSC}$: self oscillation frequency)